EE 505

Lecture 17

Current Steering DACs

Dynamic Current Source Matching

Charge Redistribution DACs

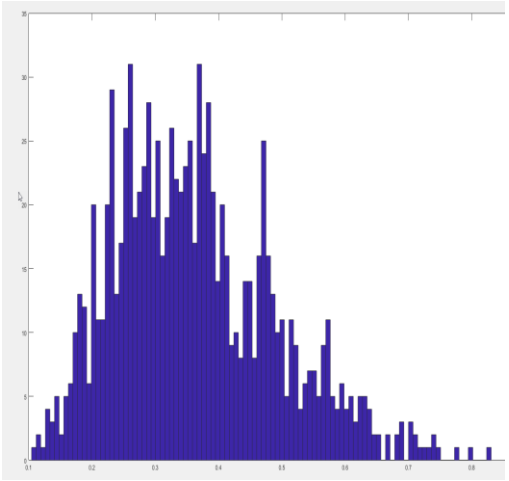
Monte Carlo Simulation Time can Become Large

Example: n=10

A_R=0.02µm
R_N=1K

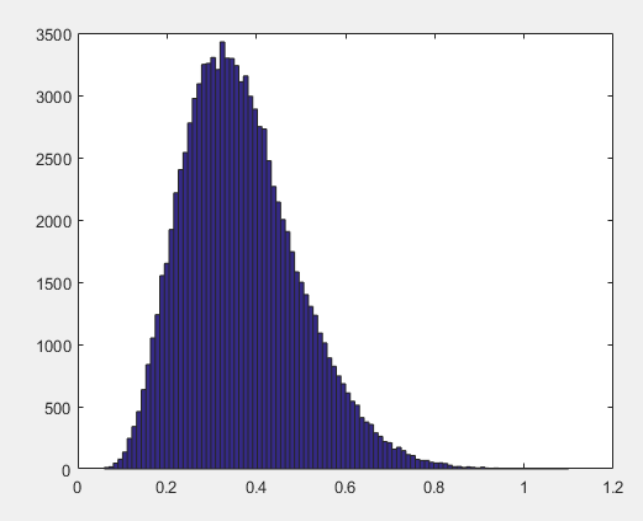
Resistor Sigma= 14.14 Ω

Binary DAC



Histogram of INL from 1000 runs

Binary DAC



Histogram of INL from 100,000 runs

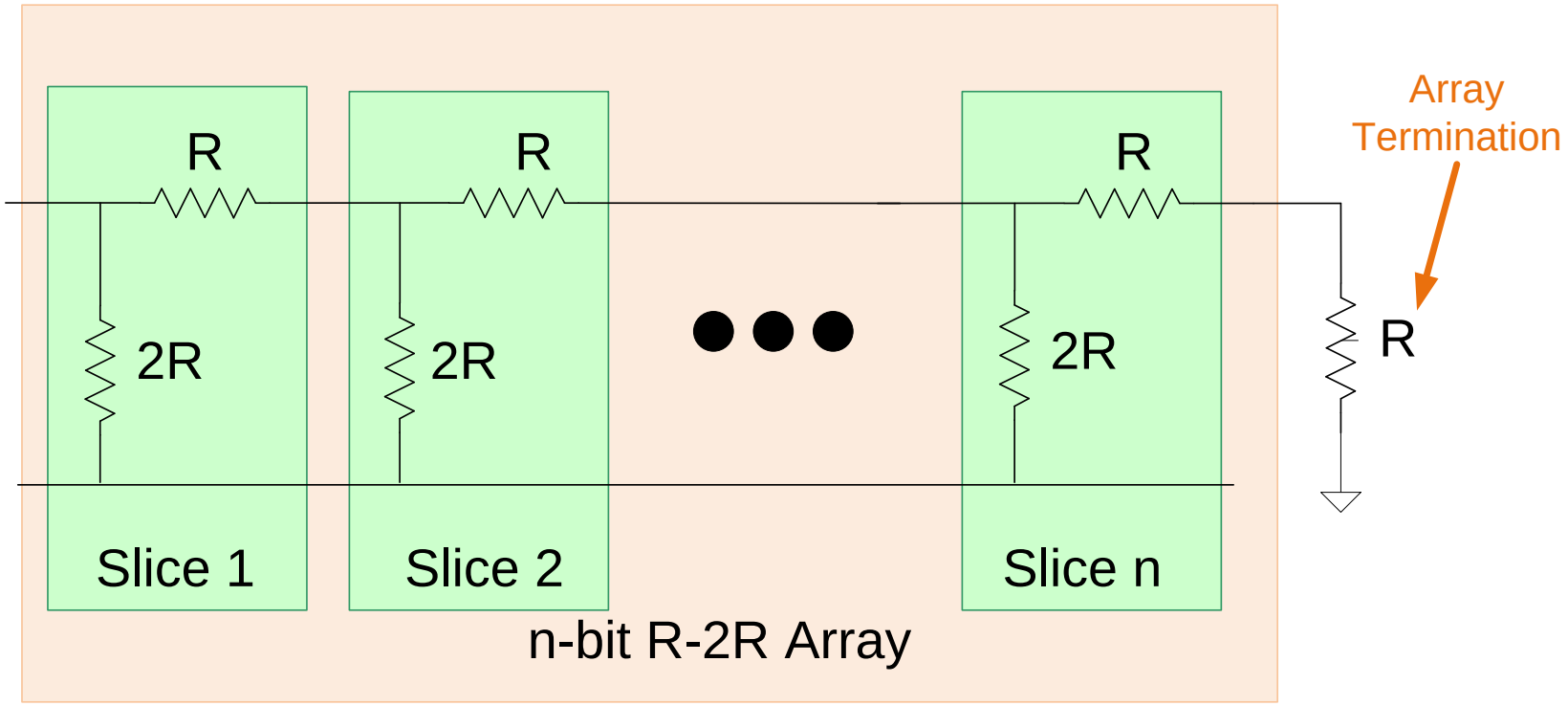
Can require a large number of runs for useful information

This should provide insight into length of Monte Carlo simulations needed to get useful results

File: BinaryWeightedDACInl.m

Review from Last Lecture

R-2R Resistor Arrays

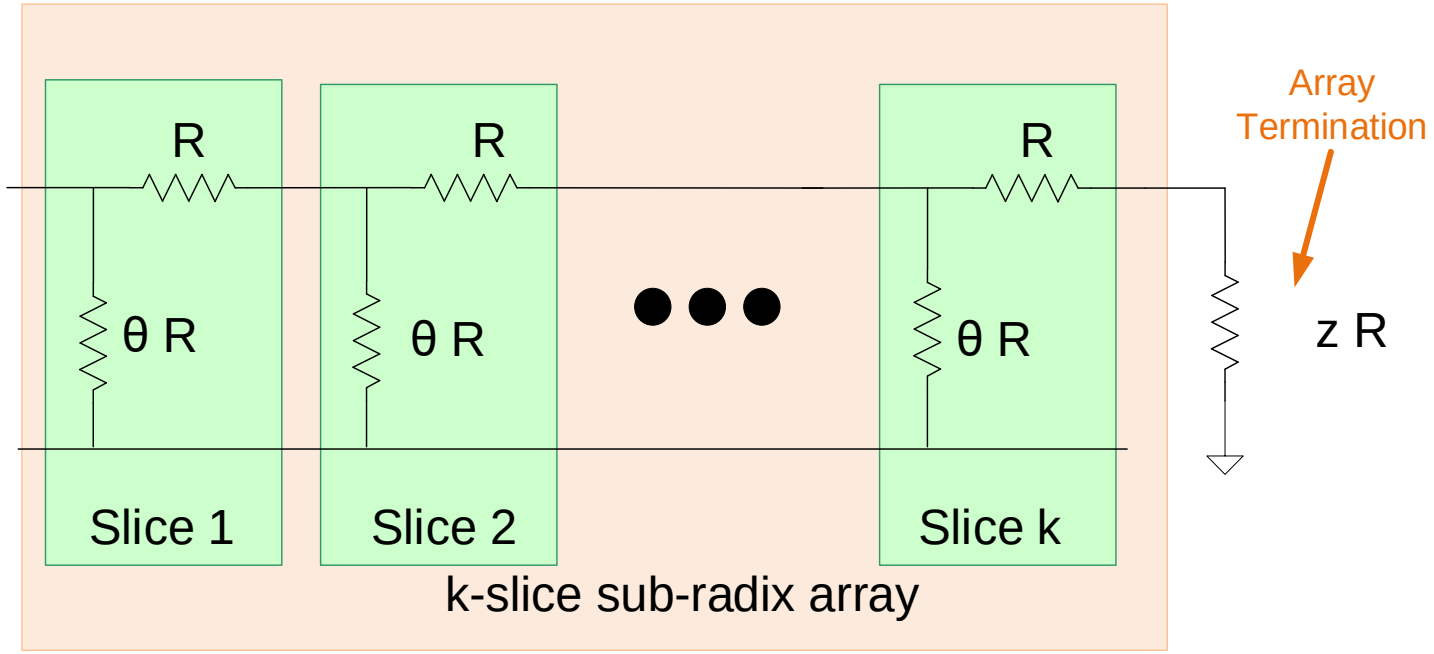


- Depicting relative resistor values (not how unary cells used)
- Conceptually, area goes up linearly with number of bit slices
- Can be used in many different ways

Review from Last Lecture

Sub-radix Array

Want Currents to Scale by 1/θ (instead of ½) from each slice to the next



Typically $2.1 < \theta < 2.5$

Termination resistor must be selected so that same attenuation is maintained

Often only the first n_1 MSB "slices" will be sub-radix

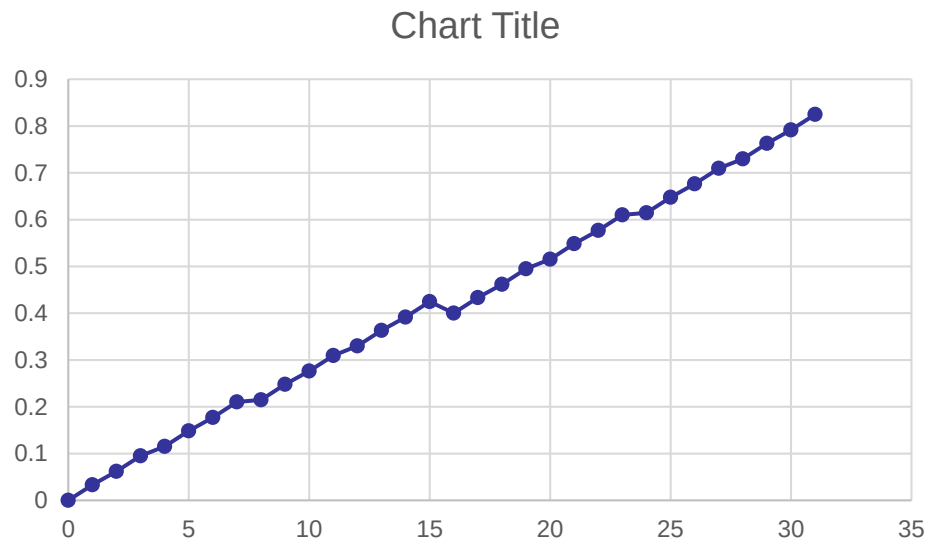
Effective number of bits when using sub-radix array will be less than k

Can be calibrated to obtain very low DNL (and maybe INL) with small area

Review from Last Lecture

Output of an optimally terminated subradix DAC of 5 bits with θ=2.5 and z=1.15831

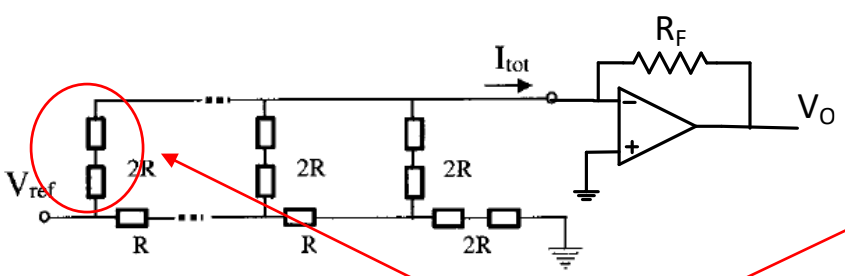
See file SubRadix DAC.xslx



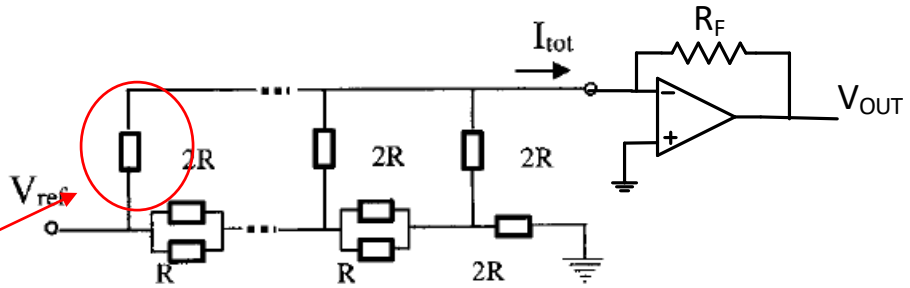
θ selected so probability of large positive gap is very small

Review from Last Lecture

Area Allocation for R and 2R Resistors



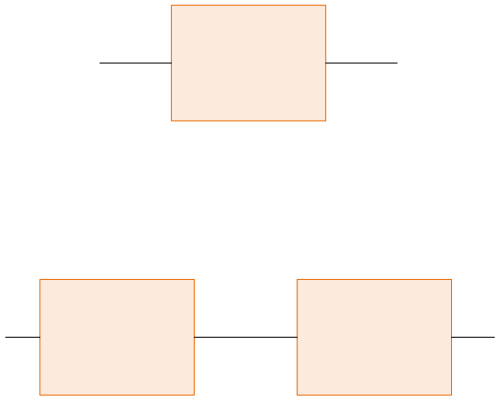
Switches not shown



Switches not shown

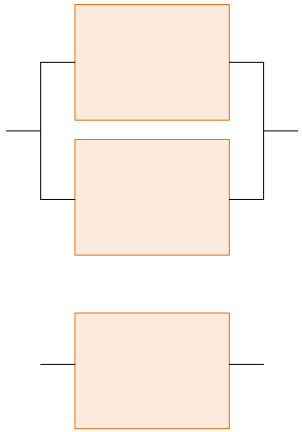
critical MSB current

Series Layout



2R Area twice R Area

Parallel Layout



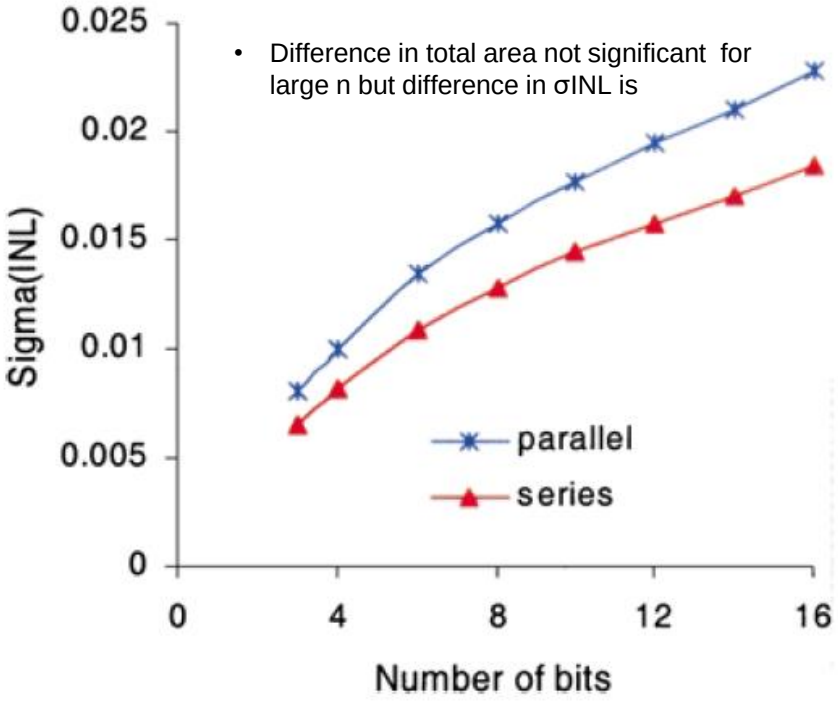
R Area twice 2R Area

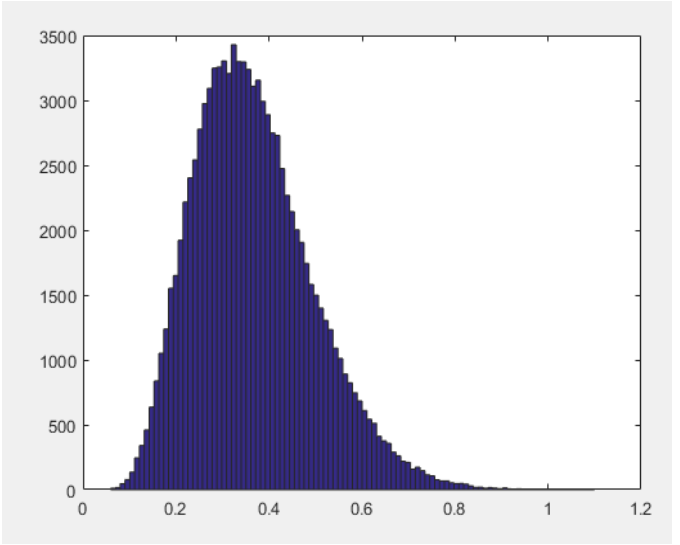
Assume area in each slice if fixed

Review from Last Lecture

Area Allocation for R and 2R Resistors

- Number of cells (and hence total area) is not constant in these simulations
- Difference in total area not significant for large n but difference in σINL is



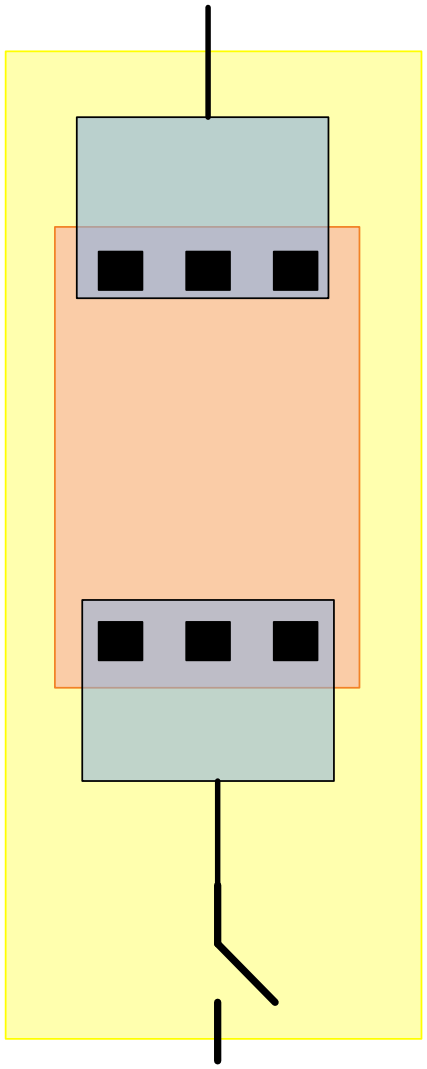


Yield is affected by both mean and standard deviation of the non-Gaussian pdf

Standard deviation of parallel layout is somewhat more (but uses less cells for n small)

Area allocation between slices also affects yield

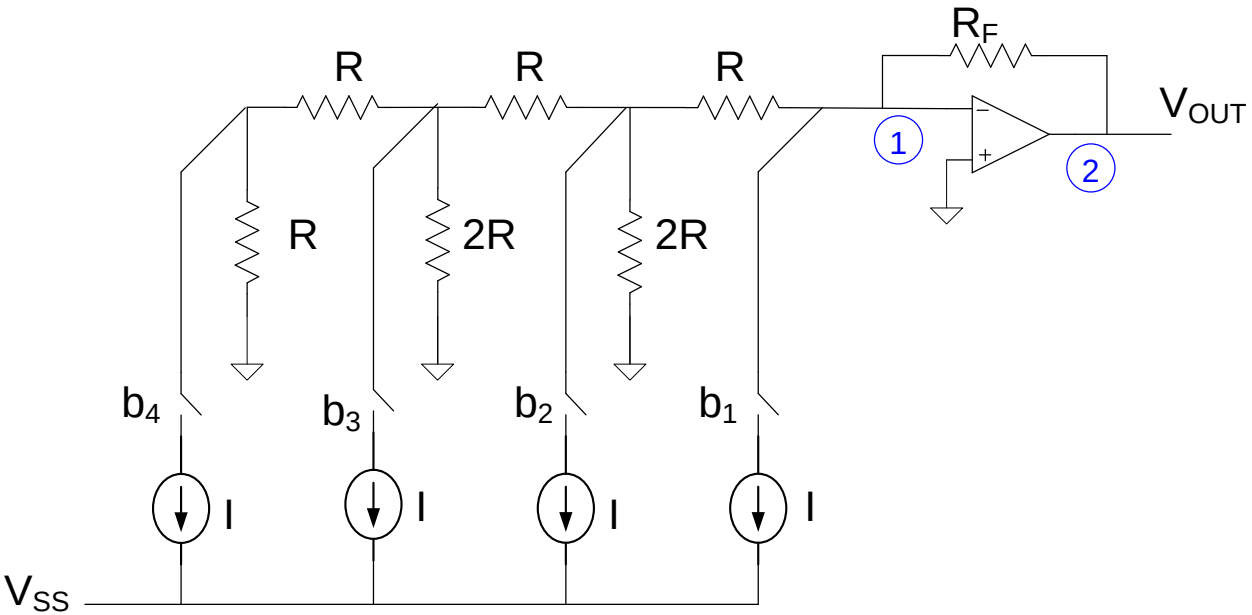
Challenges with all R-based DACs



- Switch Impedance
- Contact Resistance
- Variability
  - Resistor
  - Contact Resistance
  - Switch Impedance
- Parasitic Capacitances

Review from Last Lecture

Another R-2R DAC



Eliminates series switch resistance when switching resistors

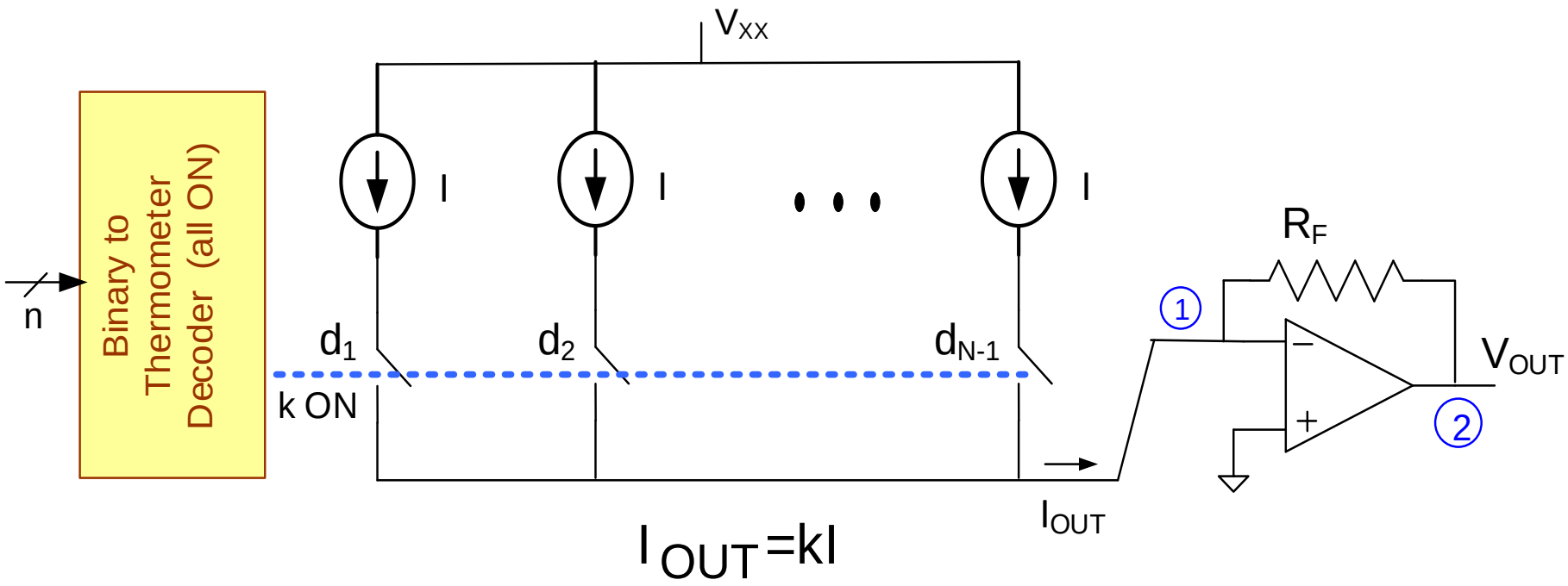
Series resistance in current source does not affect current

Must match both resistors and current sources

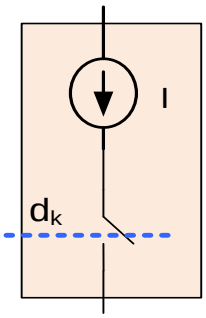
Current flow will pull capacitance on switch nodes to low before current sources leave saturation

Current flow will change power dissipation based upon digital code

Current Steering DAC



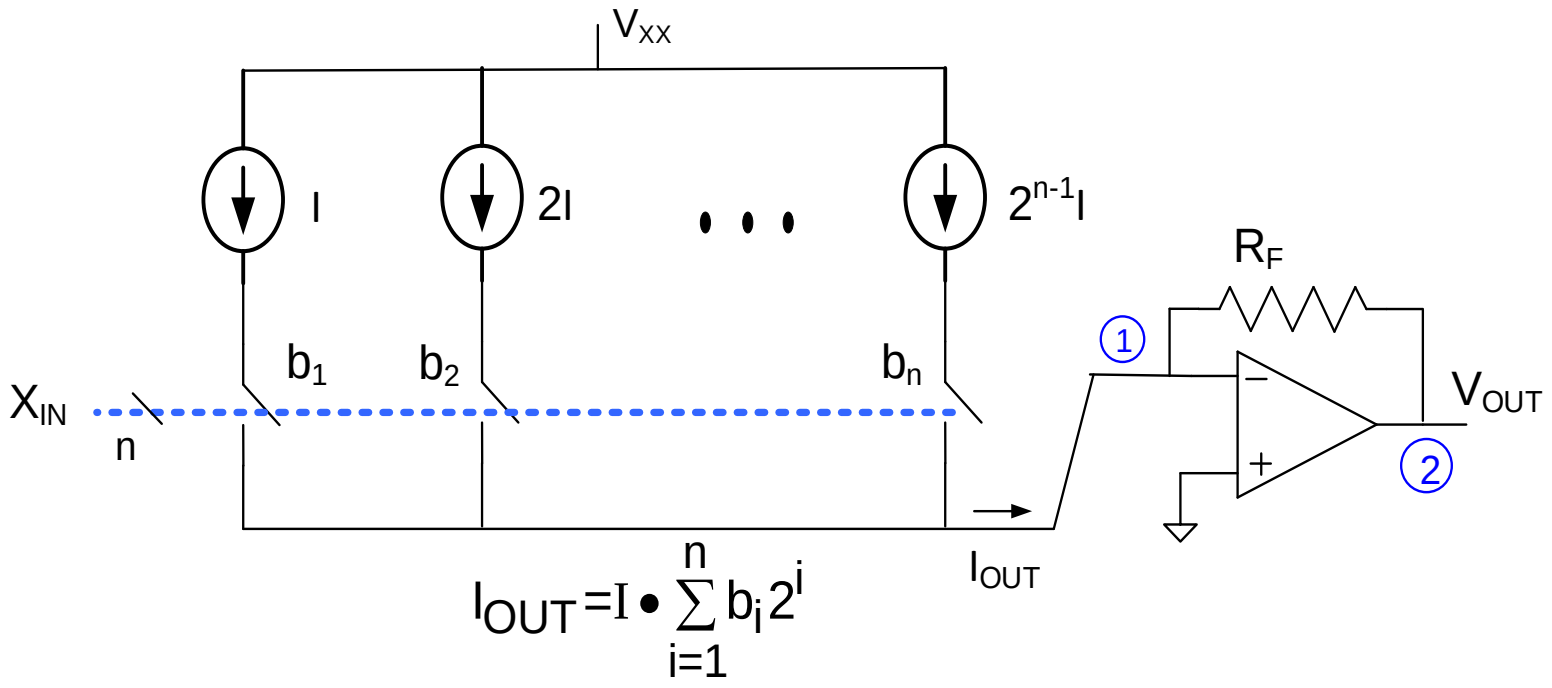
$$I_{OUT} = kI$$



Unary Slice Cell

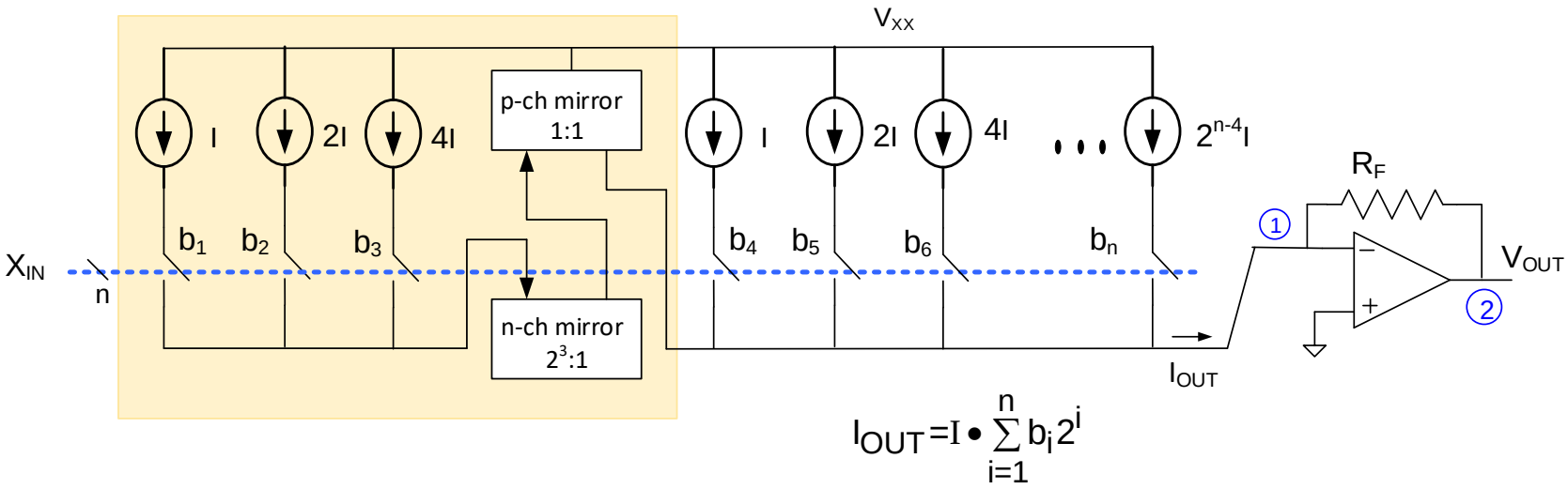
- Switch impedance of little concern
- Bottom-plate switching
- Low DNL
- Decoder impractical for large n

Current Steering Binary DAC



- eliminates decoder
- DNL not good for large n
- area ratio from MSB source to LSB source too large for large n (can make I only so small)

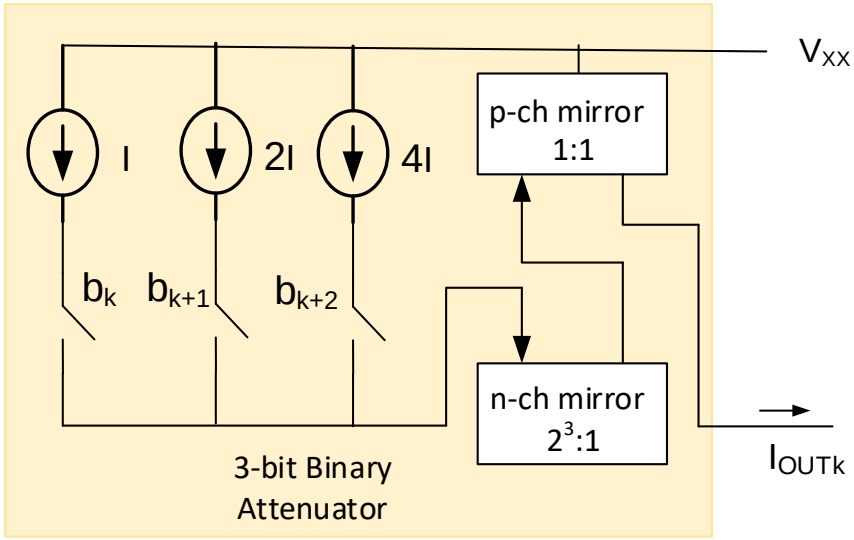
Current Steering Binary DAC

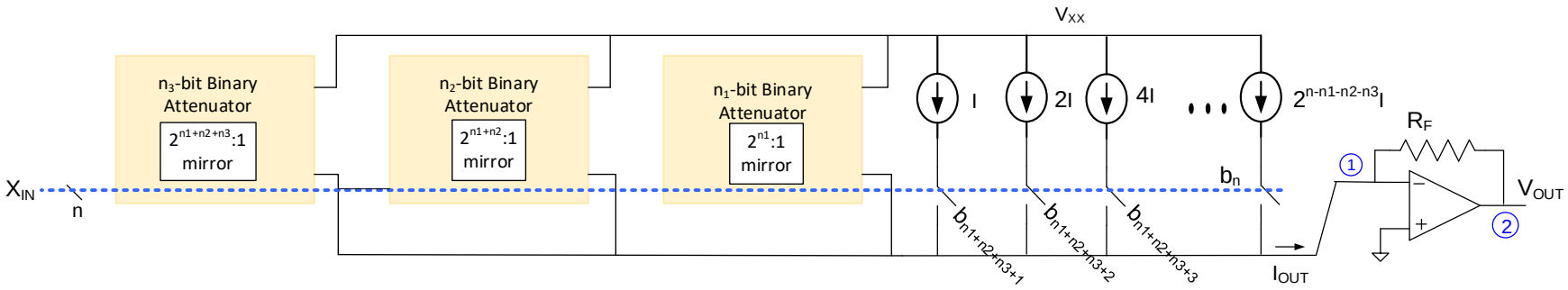


- reduces total current spread of bit cells
- reduces total number of bit cells (since cells are bundled)
- can repeat mirror current attenuator
- can change number of bits in each current attenuator stage
- Scale currents down in LSB portion rather than scale current up in MSB portion

How is performance affected by reducing the number of unary cells?
Is too much area allocated to the LSB cells?

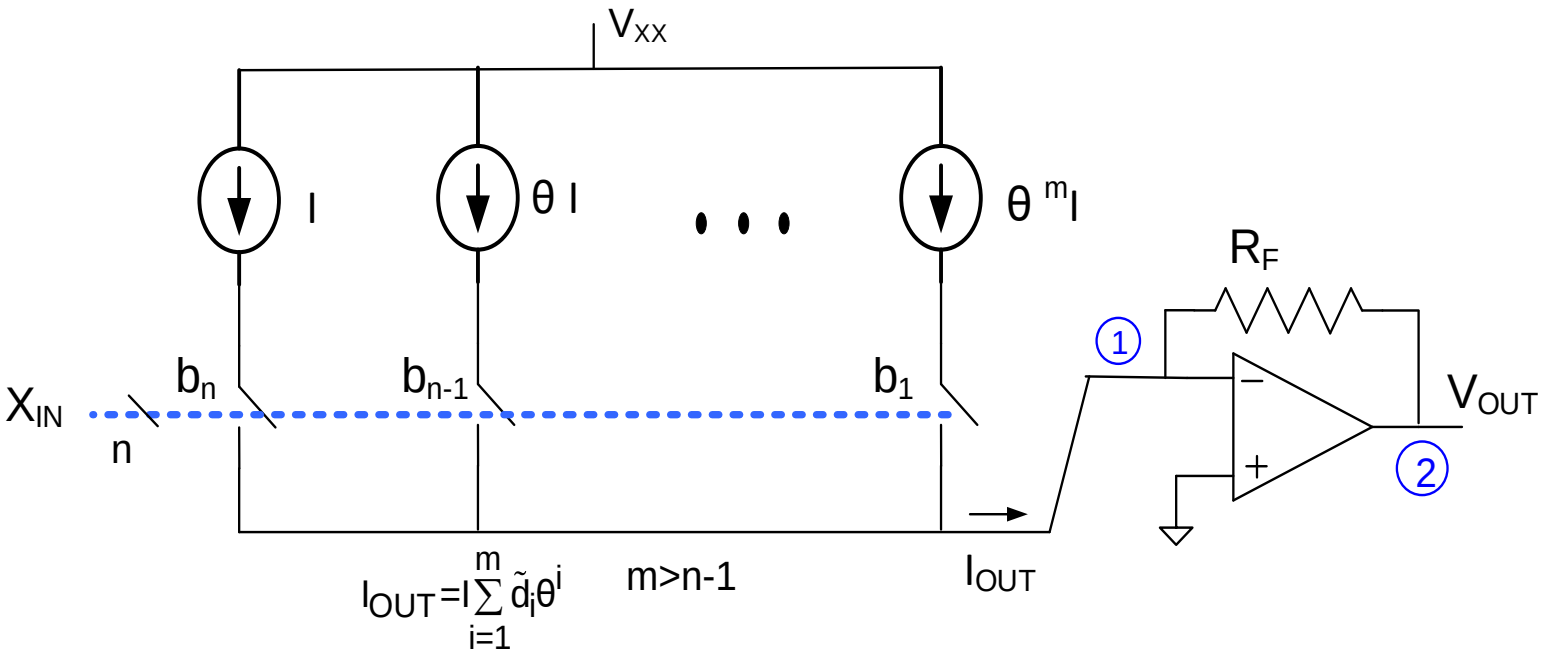
Current Steering Binary DAC





- LSB performance not critical
- Limit number of binary attenuators to avoid accumulating too much error

Sub-Radix Current Steering DAC

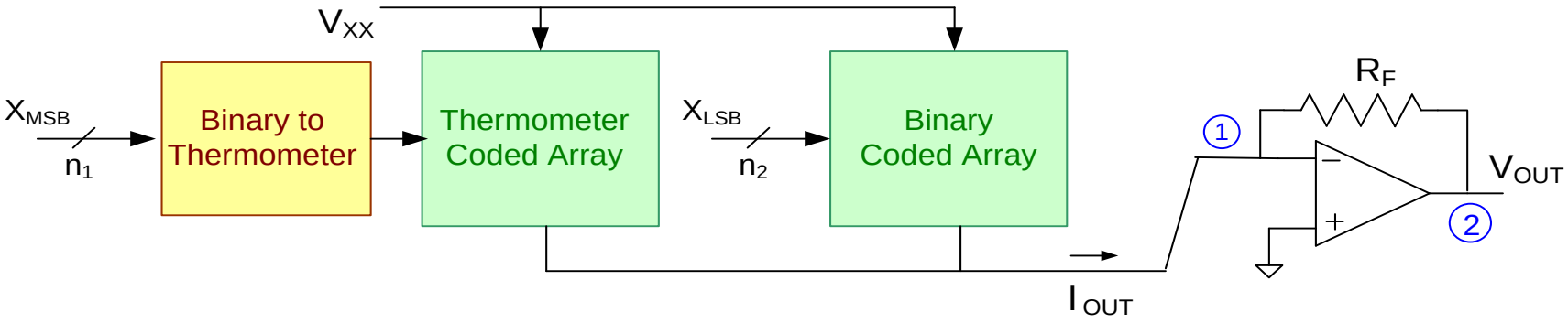


Typically $1.9<\theta<1.99$ (Depending on ratio-matching accuracy of current sources)

Takes smaller steps so takes more steps to cover range

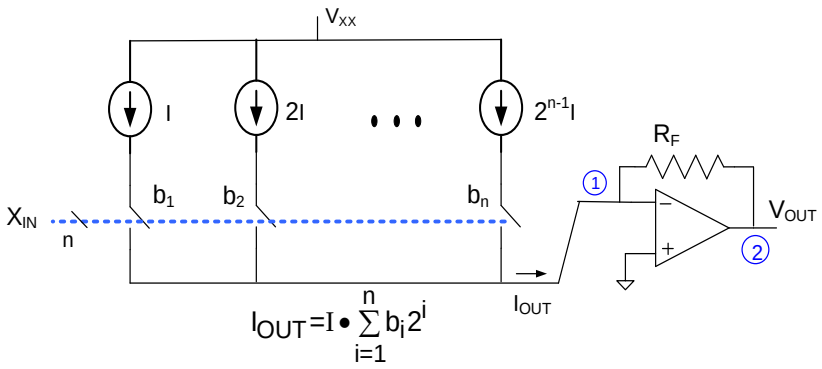
Current Steering DAC

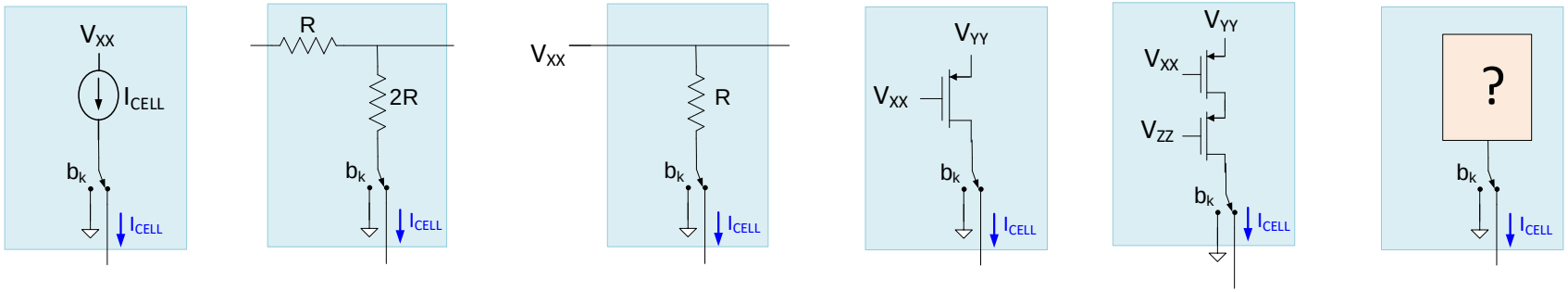
Segmented Structure Widely Used



- Binary code LSBs to reduce Decoder Complexity
- Thermometer Code MSB to manage DNL
- Partitioning between Thermometer and Binary Coding is critical

What Cells Are Used for Current Steering DAC





- What characteristics are important in a given process ?

  R_{OUT}? Speed?

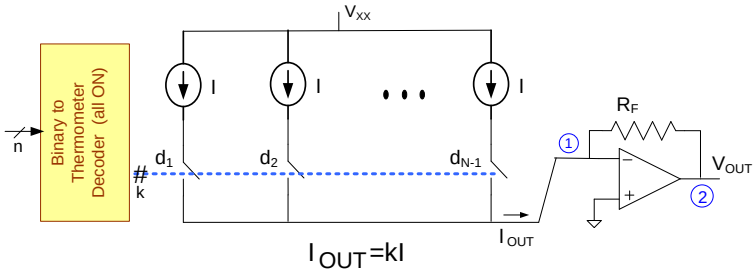
  Matching? Power ?

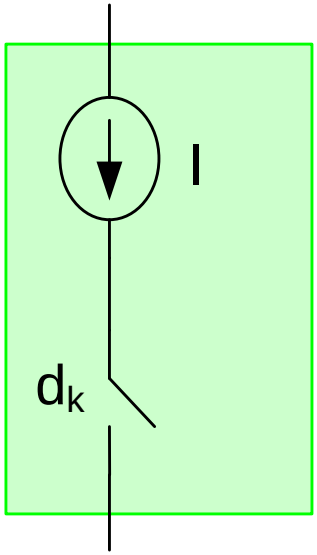
  Area (cost) ? Linearity ?

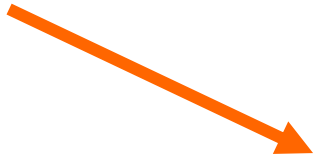
- What cells are used ?

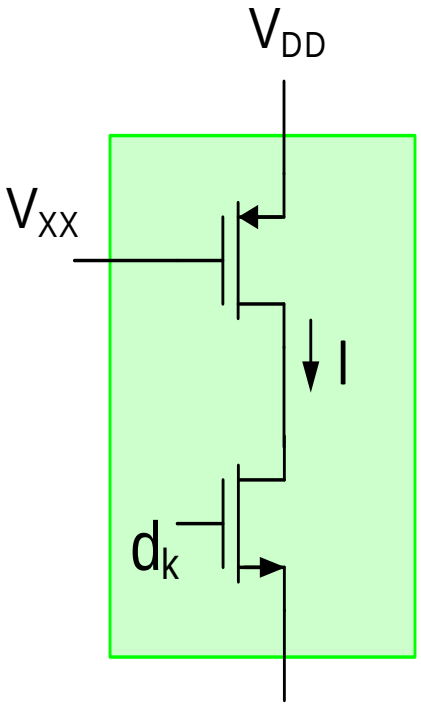
Current Steering DAC

Current Source Bit Cells:









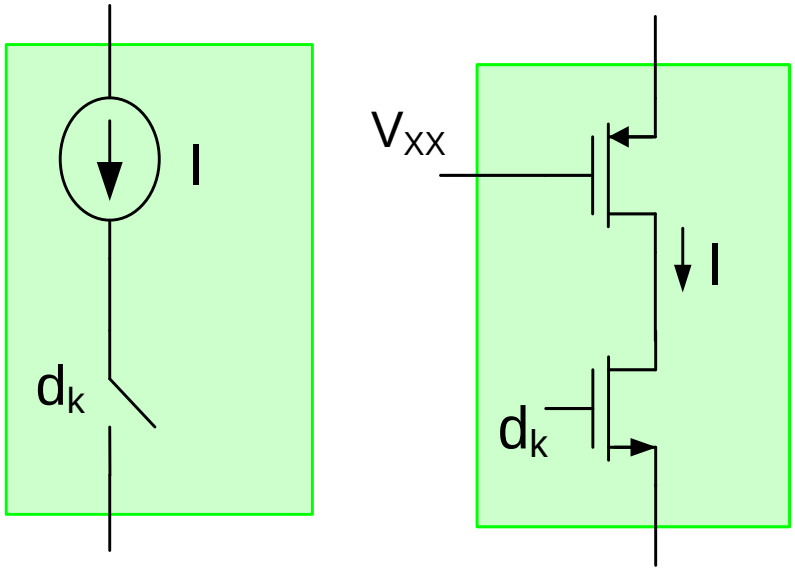
Bottom plate switching

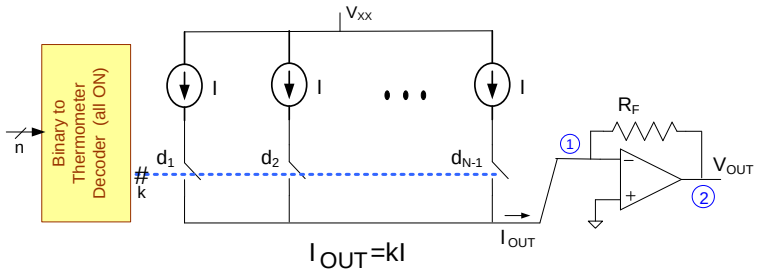
Is output impedance of current sources of concern?

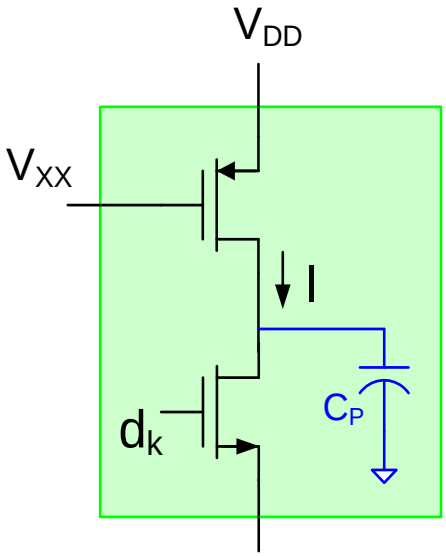
No ! Matching is important but linearity is not

Current Steering DAC

Current Source Bit Cells:



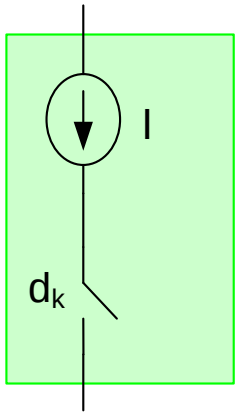


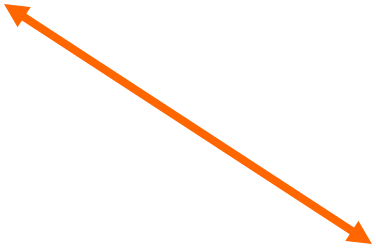


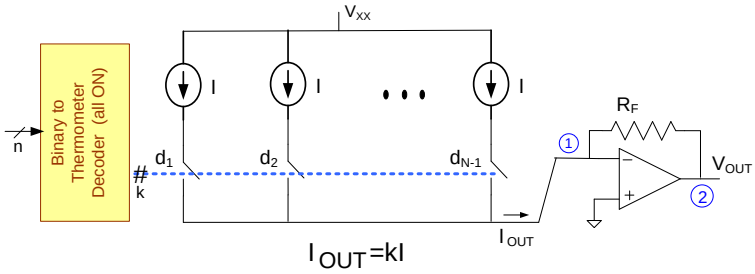
Parasitic capacitance will charge to V_{XX} before current source saturates

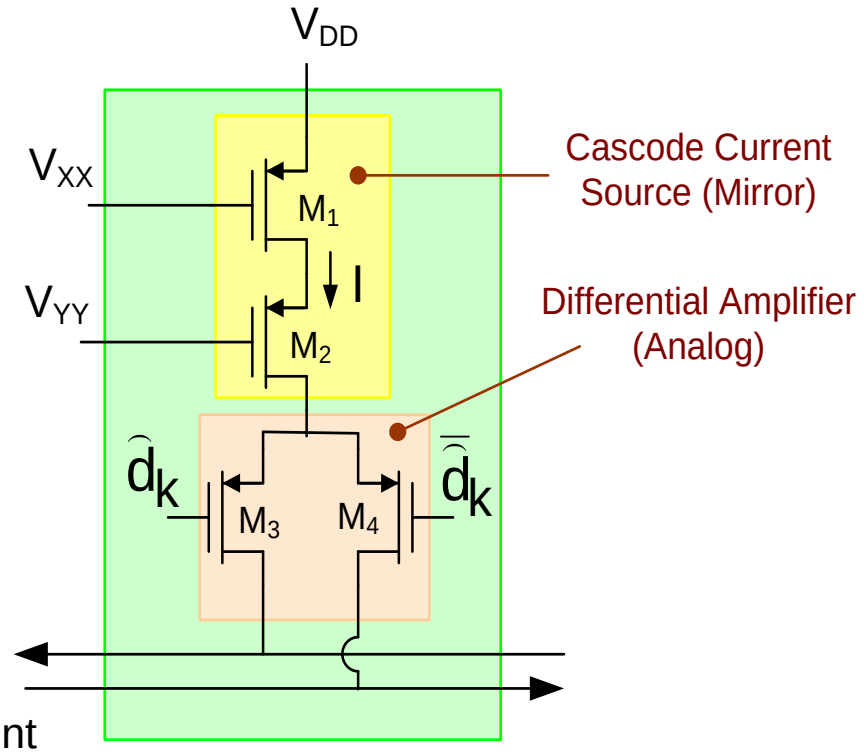
Power dissipation is code dependent

Current Steering DAC



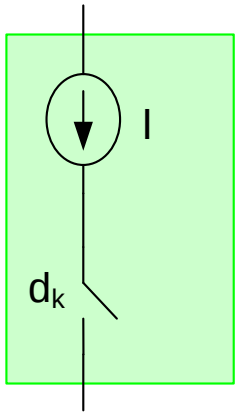


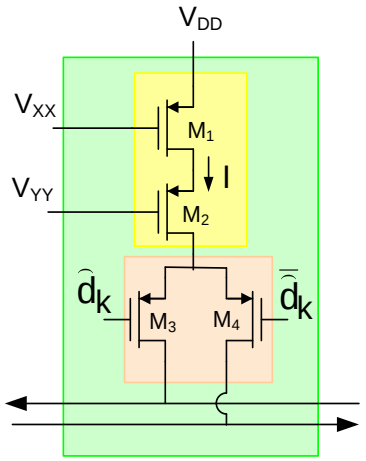


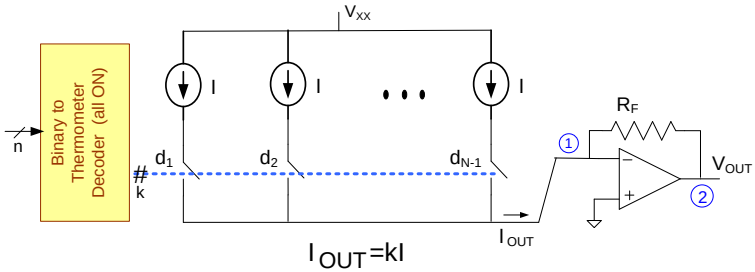


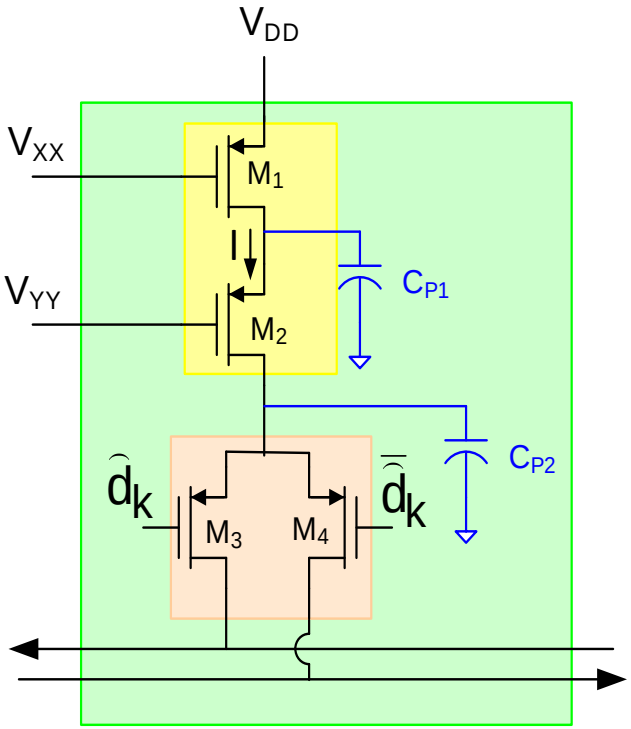
- Current steering instead of current switching
- Power dissipation in current sources remains constant
- Smaller gate voltages can be used to steer current
- Dump current can provide differential DAC output

Current Steering DAC



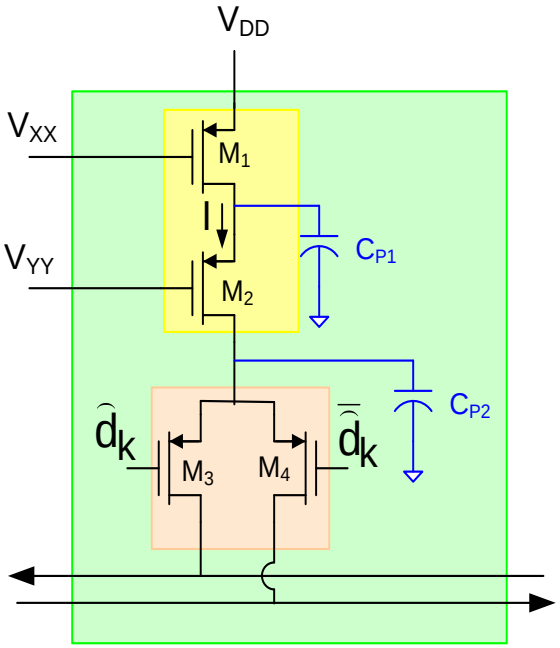


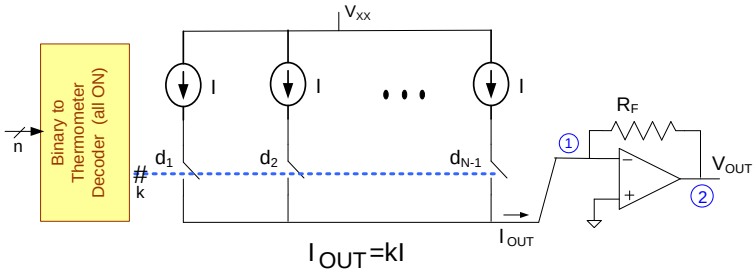


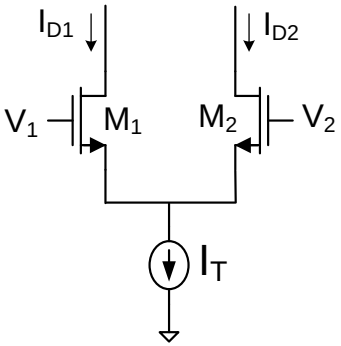


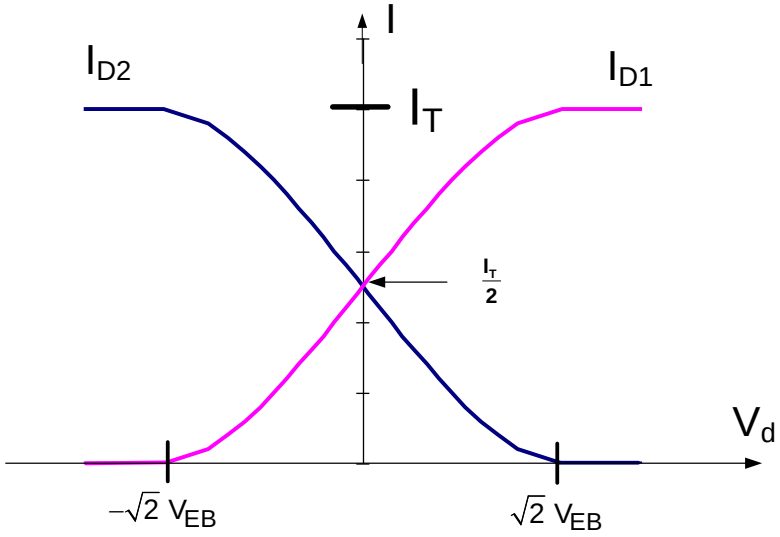
- Parasitic capacitances do not charge and discharge
- Current steering provides inherent cascoding
- This structure is a double-cascode

Current Steering DAC





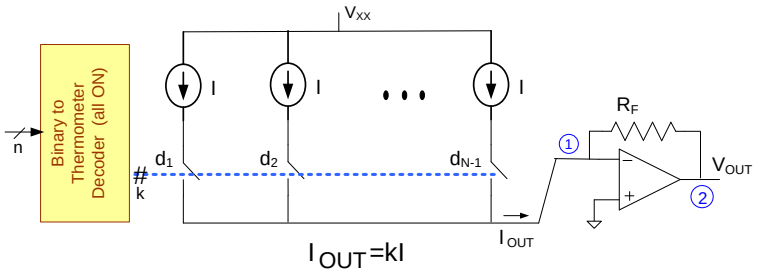


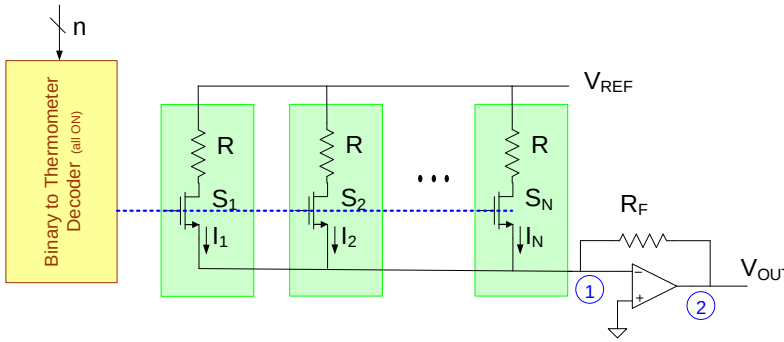


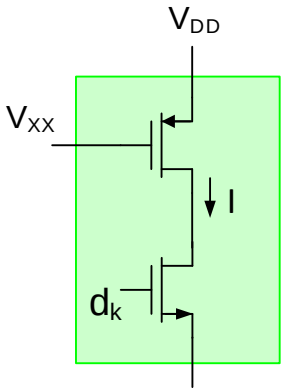
Signal swings only need to be large enough to steer current

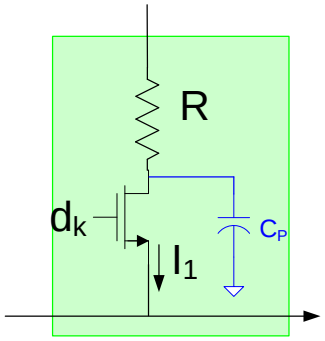
Current Steering DAC Comparison

Current-source bit vs Resistor-Based Bit Cell





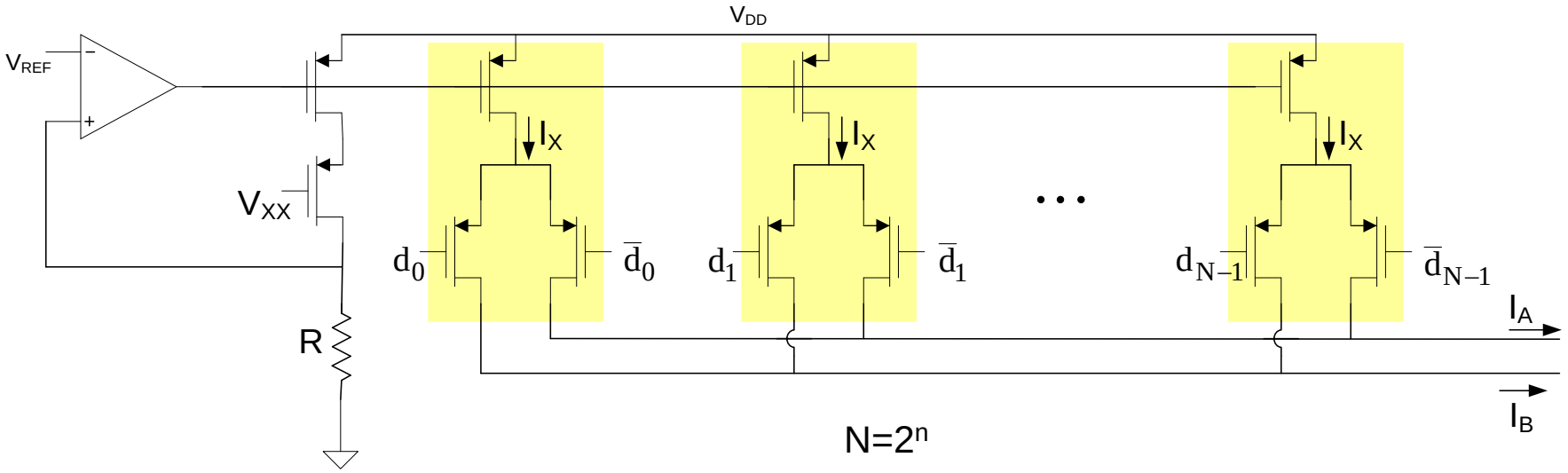




Do current-source bit cells also introduce code-dependent β in the feedback amplifier and thus code-dependent op amp settling?

No! β=1 for all codes with current-source bit cell.

Current Steering DAC with Supply Independent Biasing



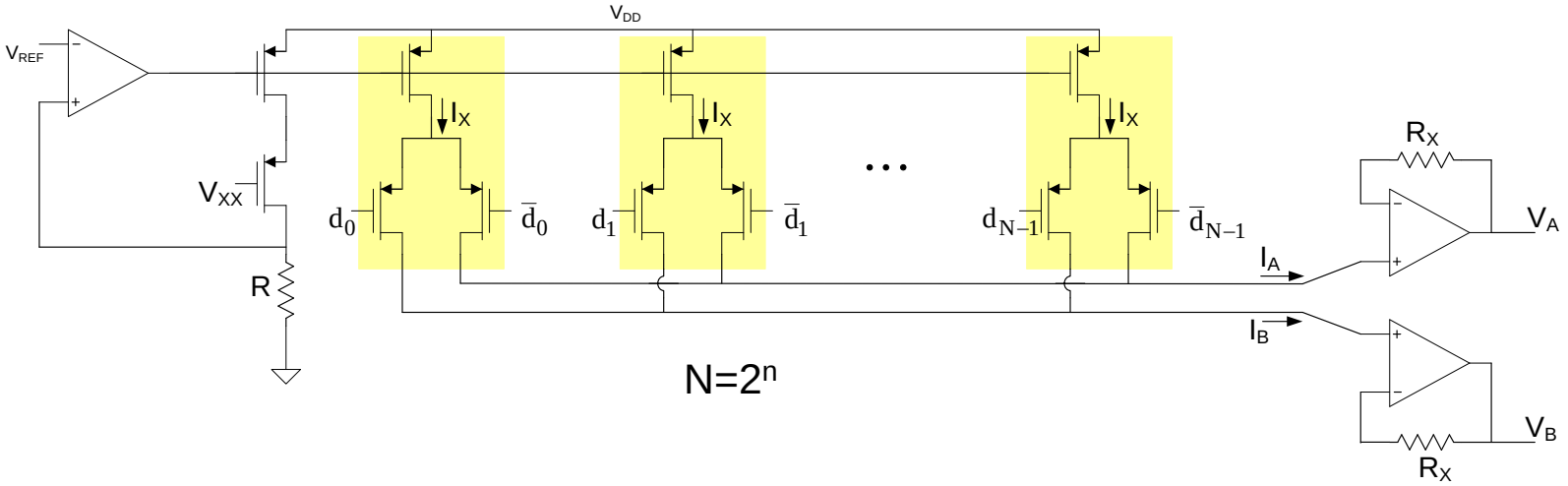
If transistors on top row are all matched, $I_X = V_{REF}/R$

Thermometer coded structure (requires binary to thermometer decoder)

$$I_A = \left(\frac{V_{REF}}{R}\right)\sum_{i=0}^{N-1} d_i$$

Provides Differential Output Currents

Current Steering DAC with Supply Independent Biasing

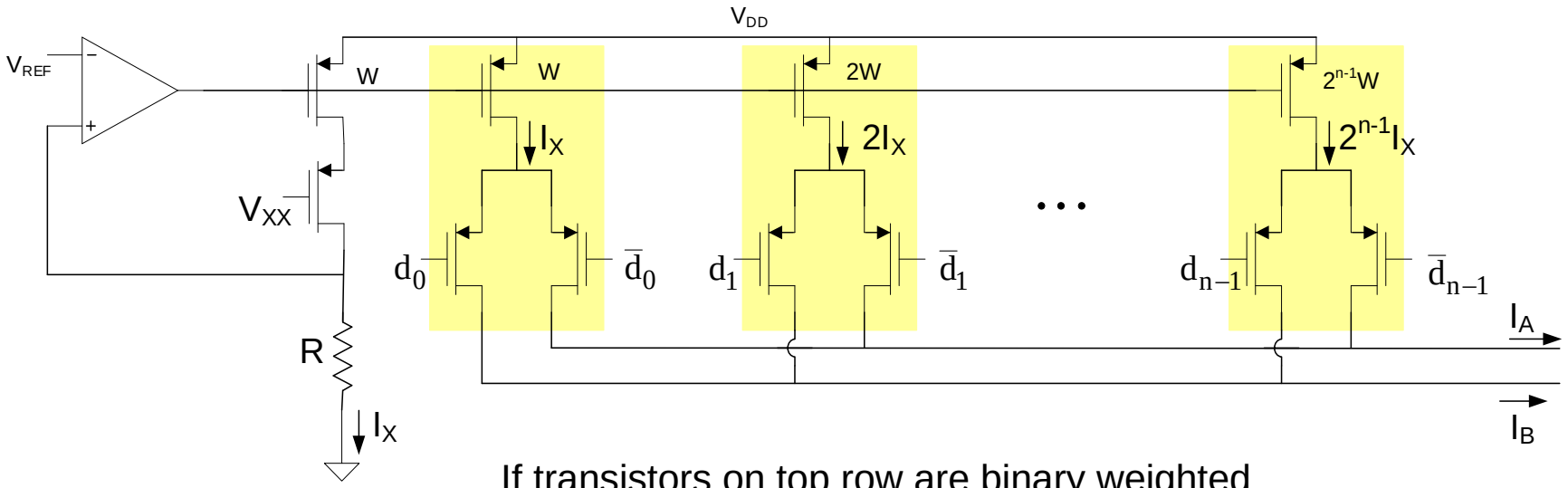


If transistors on top row are all matched, $I_X = V_{REF}/R$

$$V_A = \left(-V_{REF} \frac{R_A}{R} \right) \sum_{i=0}^{N-1} d_i$$

Provides Differential Output Voltages

Current Current Steering DAC with Supply Independent Biasing



If transistors on top row are binary weighted

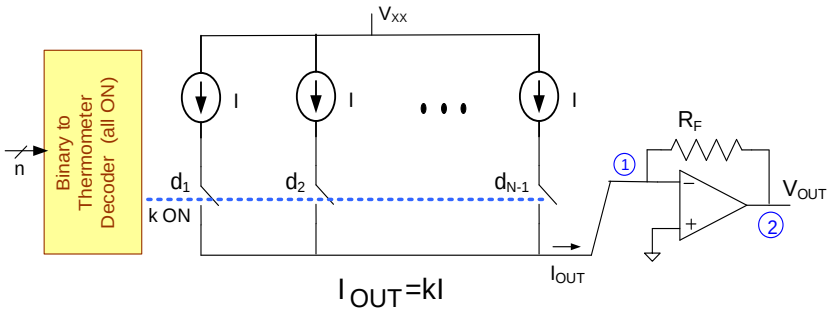
$$I_A = \left(\frac{V_{REF}}{R}\right)\sum_{i=0}^{n-1}\frac{d_i}{2^{n-i}}$$

Provides Differential Output Currents

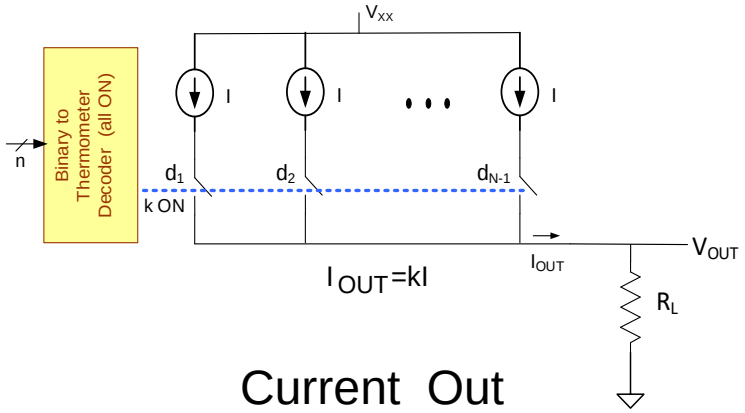
Will usually use parallel connections of unary transistor cells to increase effective W

Does this serve as an MDAC?

Current Steering DAC



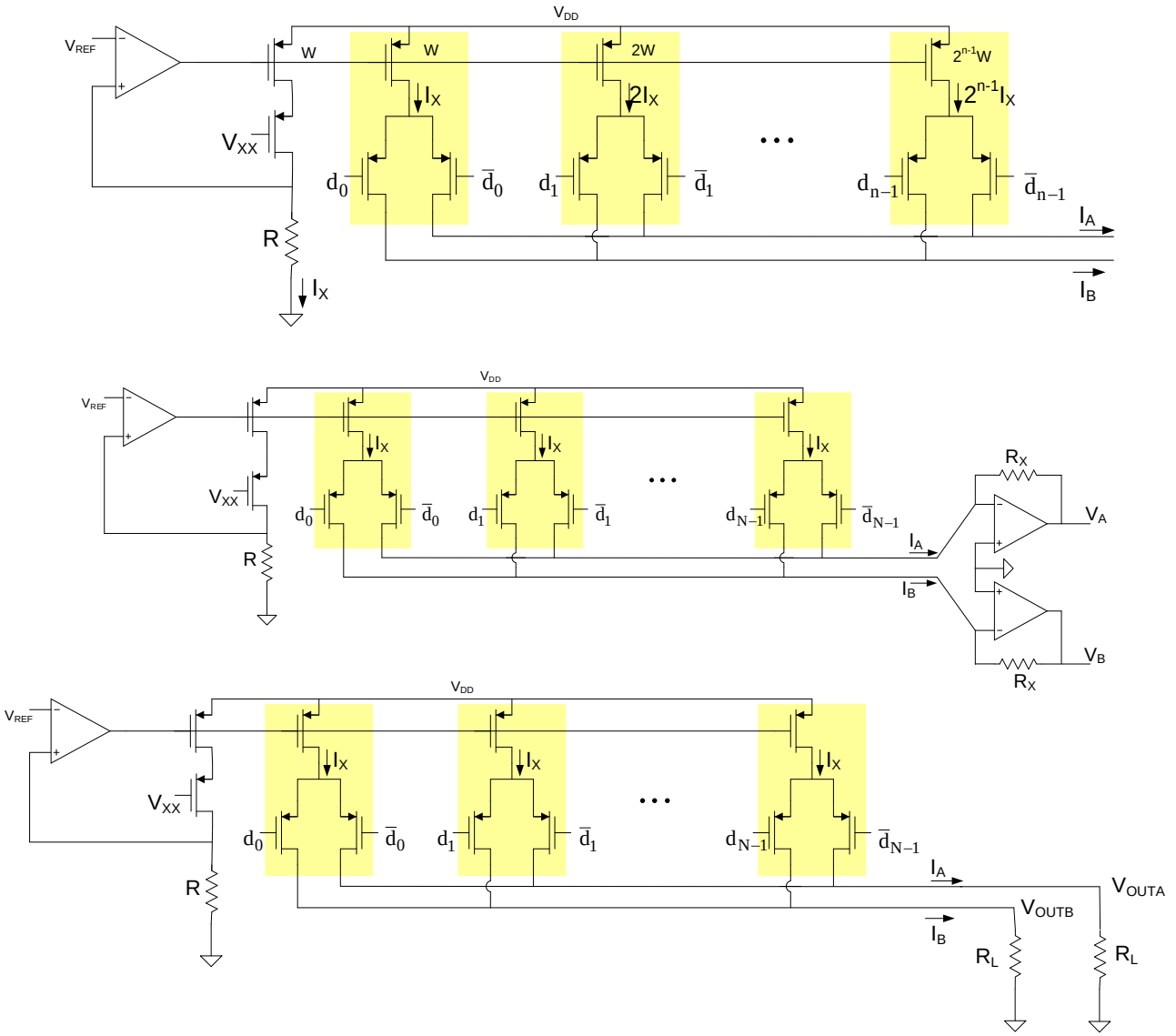
Voltage Out



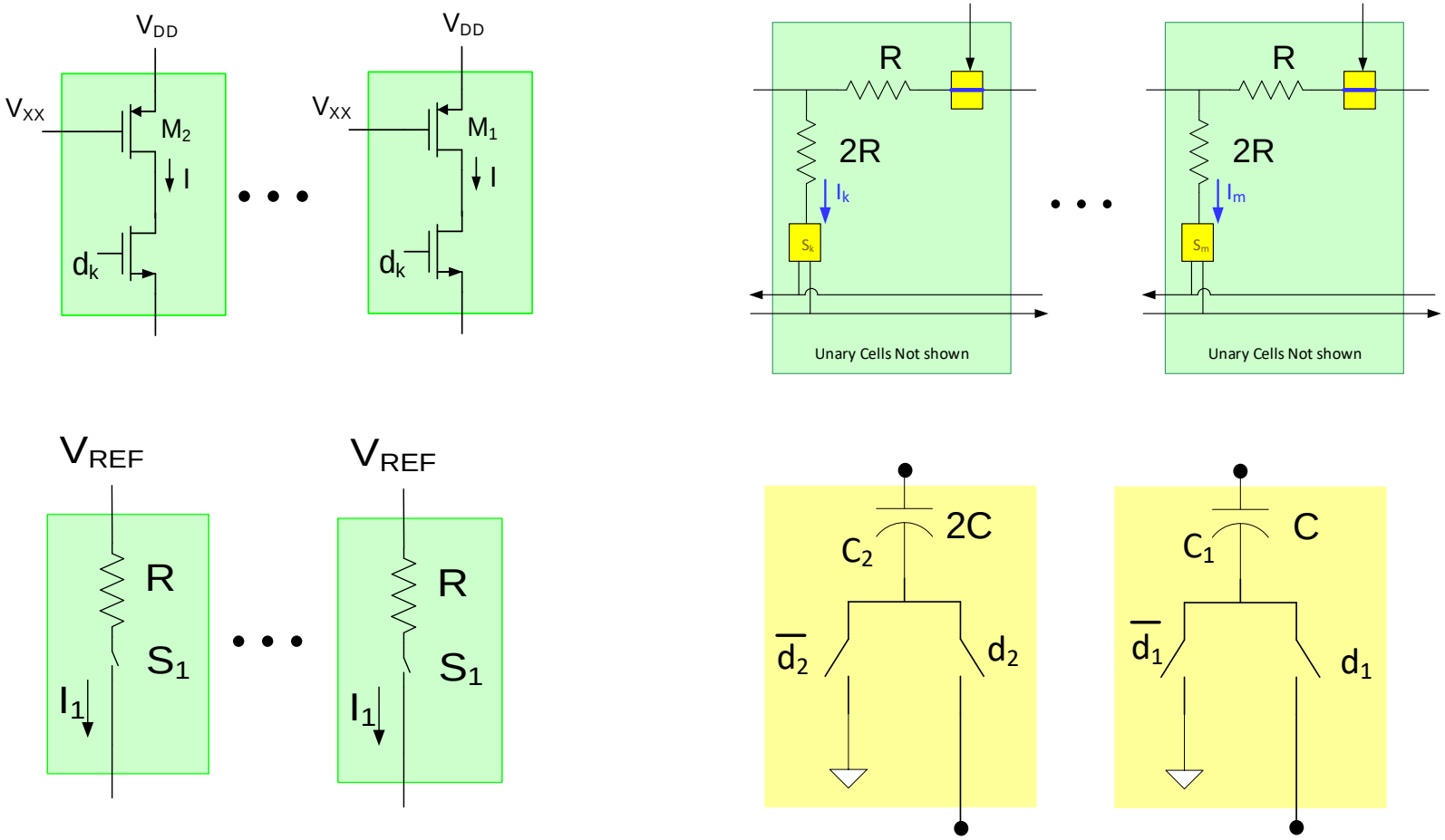
Current Out

- Many current steering DACs have an output current instead of an output voltage
- Output voltage is often established by steering current to a fixed external resistor (50Ω or 100 Ω)
- Most basic current steering architectures with a high output impedance can be used by simply removing the op amp
- Whereas output impedance of current sources was not of major concern when driving a null-port, it can be of major concern for current output
- Speed may improve and power dissipation may decrease in internal circuitry if output is current

Current Steering DAC with current output, buffered output, resistor load



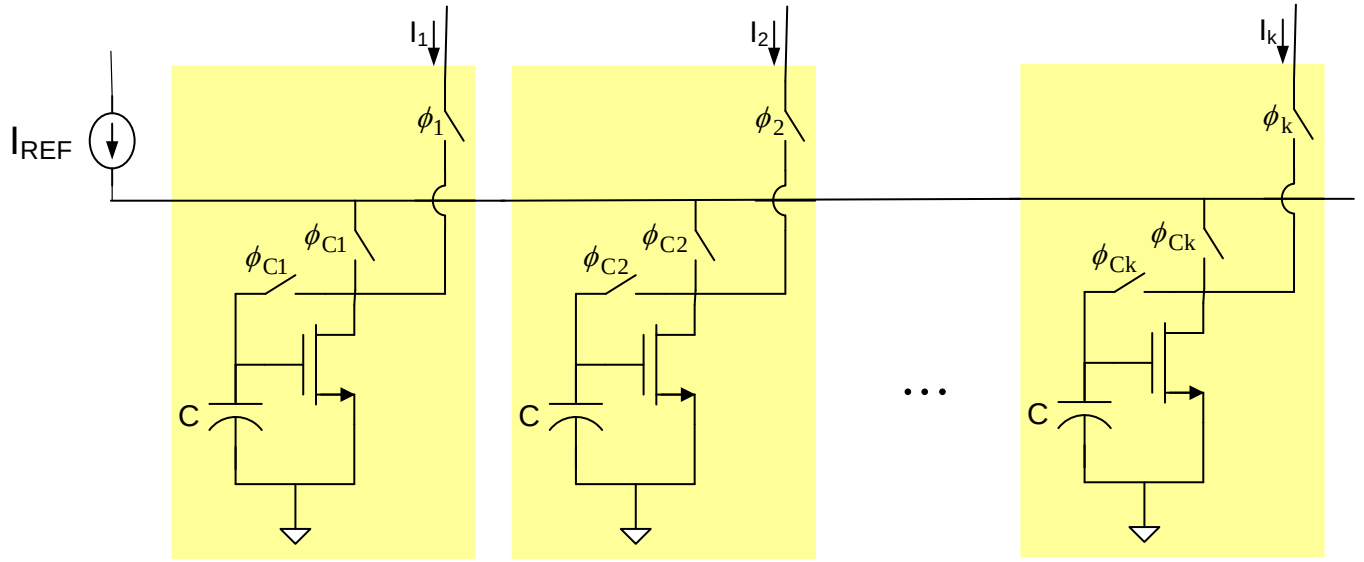
Matching is Critical in all DACs Considered



Obtaining adequate matching remains one of the major challenges facing the designer!

Choice of most practical bit cell may be strongly dependent upon matching characteristics in a specific process (relative value of Pelgrom parameters)

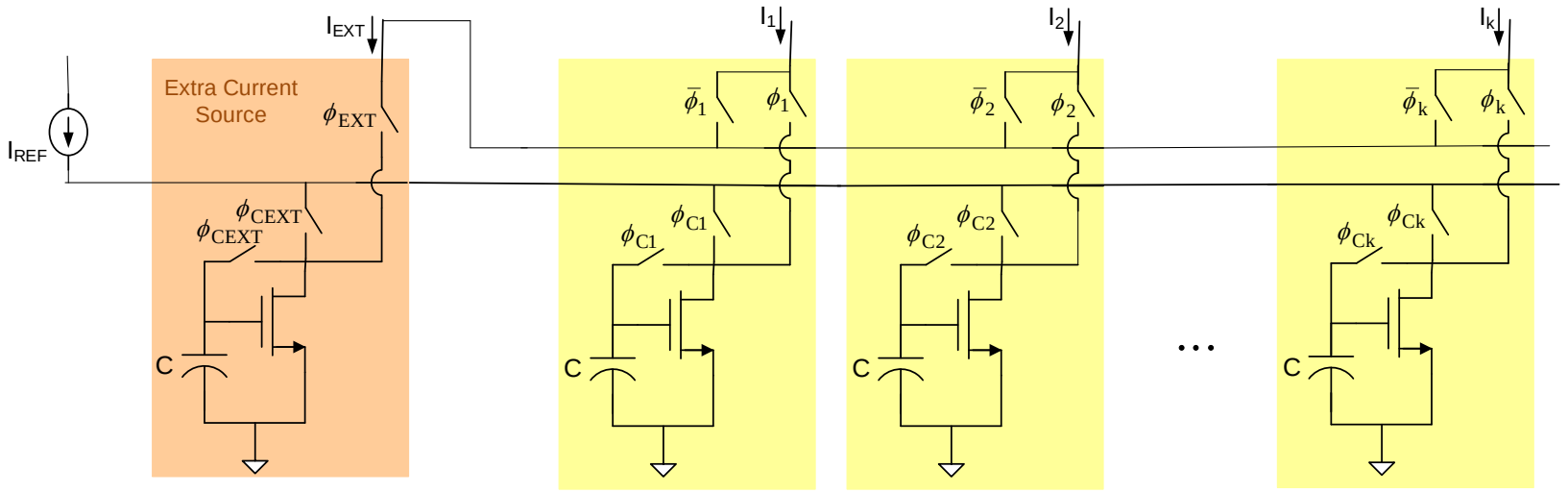
Dynamic Current Source Matching



- Correct charge is stored on C to make all currents equal to I_{REF}
- Does not require matching of transistors or capacitors
- Requires refreshing to keep charge on C
- Form of self-calibration
- Calibrates current sources one at a time
- Current source unavailable for use while calibrating
- Can be directly used in DACs (thermometer or binary coded)
- Still use steering rather than switching in DAC

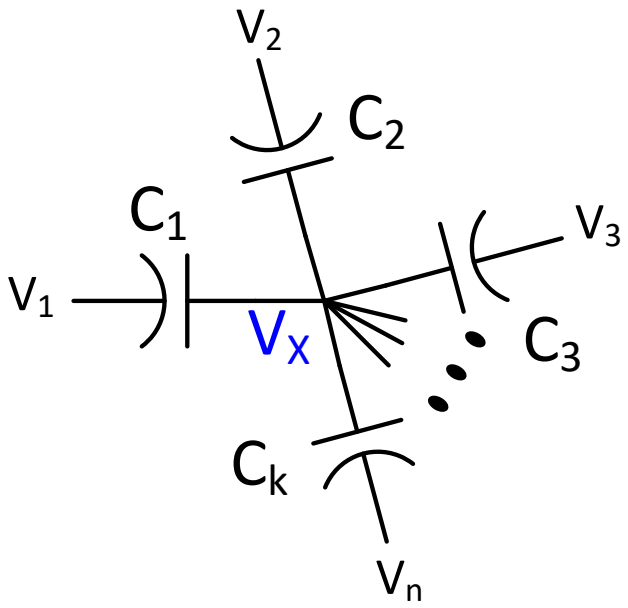
Often termed “Current Copier” or “Current Replication” circuit

Dynamic Current Source Matching



Extra current source can be added to facilitate background calibration

Charge Redistribution Principle



$$\sum_{i=1}^{k} C_i \left(V_k - V_X \right) = Q_X$$

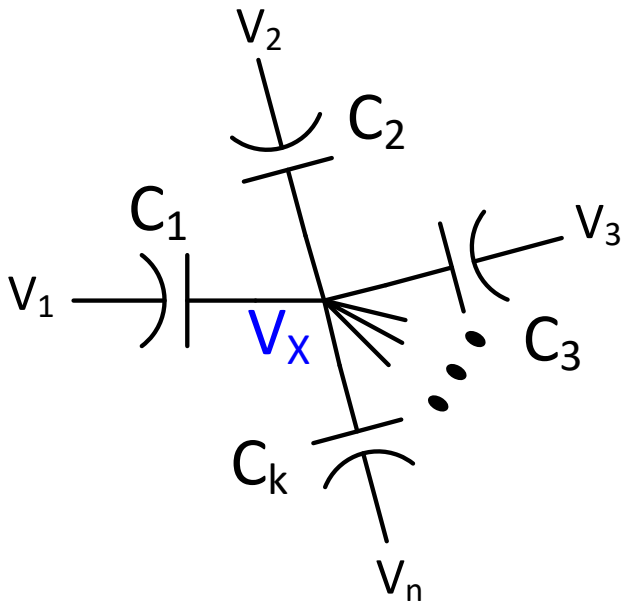
Charge on capacitors is preserved if there is no loss element on any of the capacitors

$$\sum_{i=1}^{k} C_i V_i - V_X \sum_{i=1}^{k} C_i = Q_X$$

Thus for any time-dependent voltages $V_1, \ldots V_k$

$$V_X = \frac{\sum_{i=1}^{k} C_i V_i - Q_X}{\sum_{i=1}^{k} C_i}$$

Charge Redistribution Principle

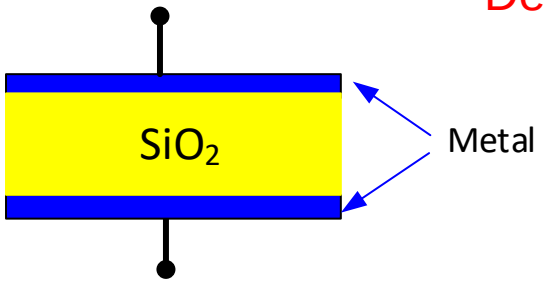


$$V_X = \frac{\sum_{i=1}^{k} C_i V_i - Q_X}{\sum_{i=1}^{k} C_i}$$

All capacitors will have some gradual leakage thus causing Q_T to change

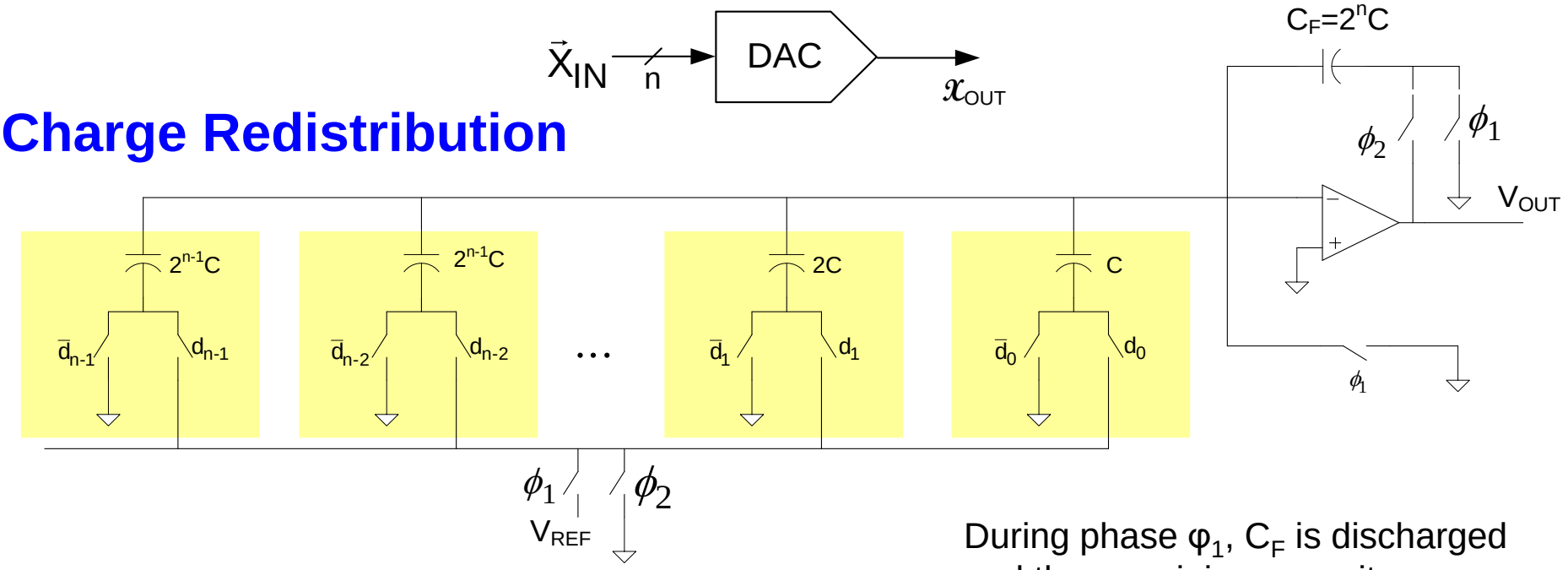
How long will charge on a simple M-SiO_2-M capacitor be retained in a standard semiconductor process?

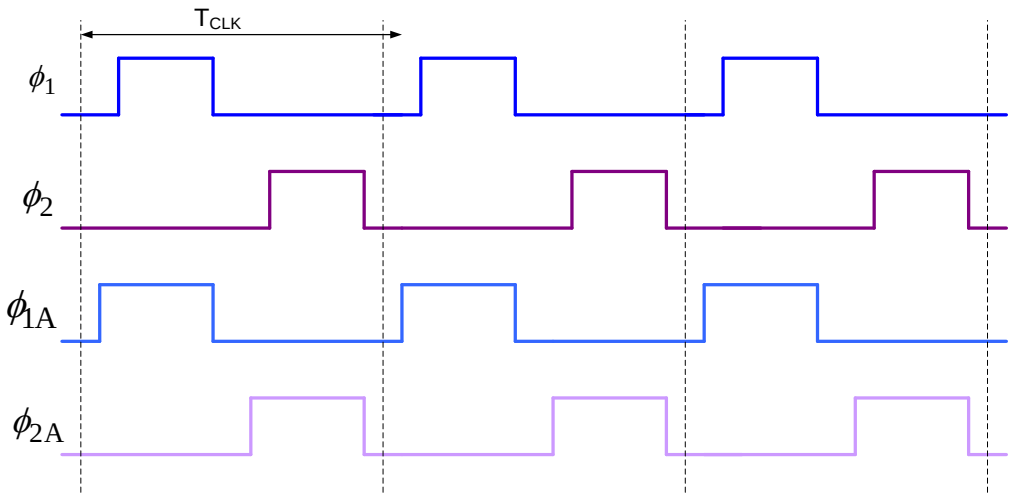
Decades !



DAC Architectures

Charge Redistribution





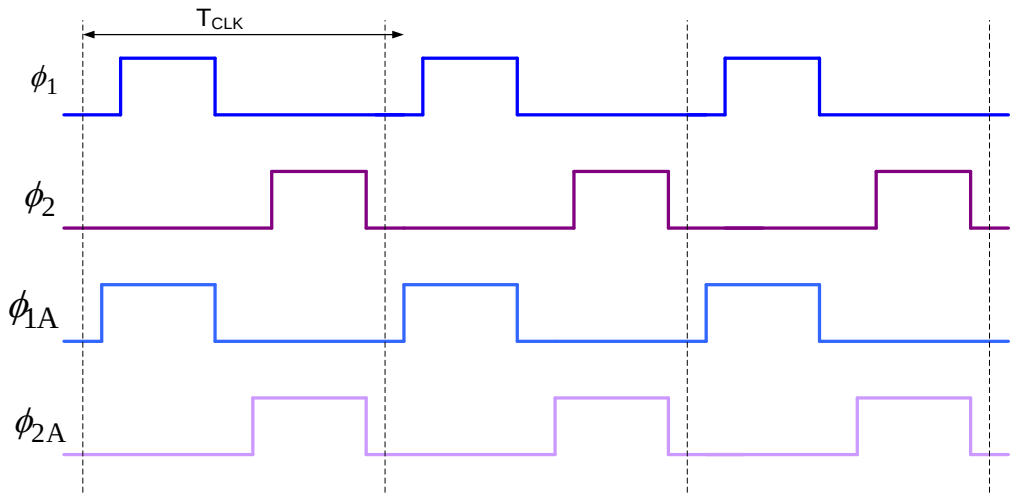
During phase φ_1, C_F is discharged and the remaining capacitors are charged to either V_{REF} or 0V depending upon Boolean input – total charge is denoted as Q_{SET}

During phase φ_2, all charge on input-connected capacitors is transferred to C_F

DAC output voltage is $V_{OUT} = \frac{Q_{SET}}{C_F}$

DAC Architectures

Charge Redistribution

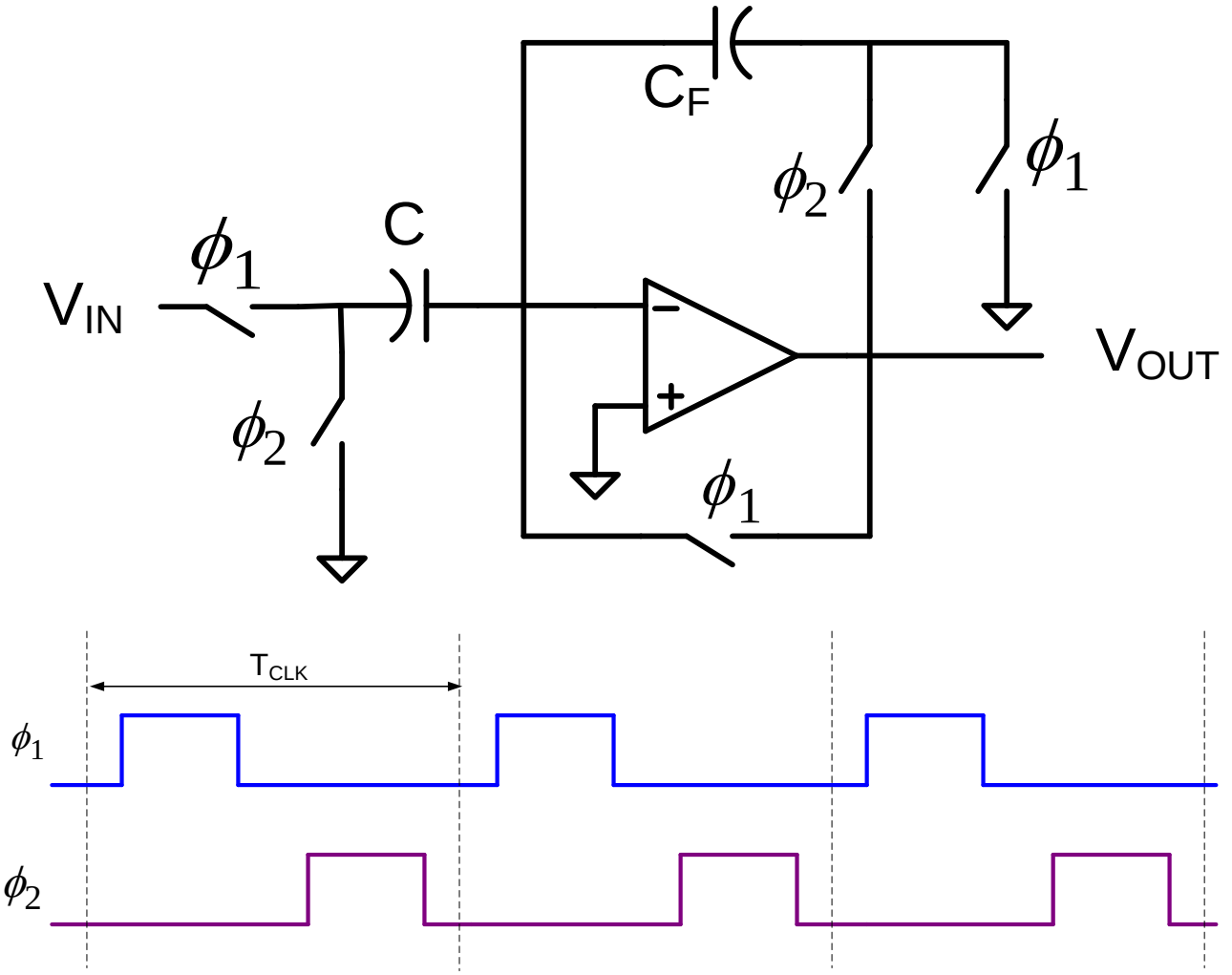


During phase φ_2, the previous output voltage is sampled on C_X

During phase φ_1, the Op Amp has feedback through C_X thus establishing a null-port at the input so voltage on selected sampling capacitors is V_{REF}

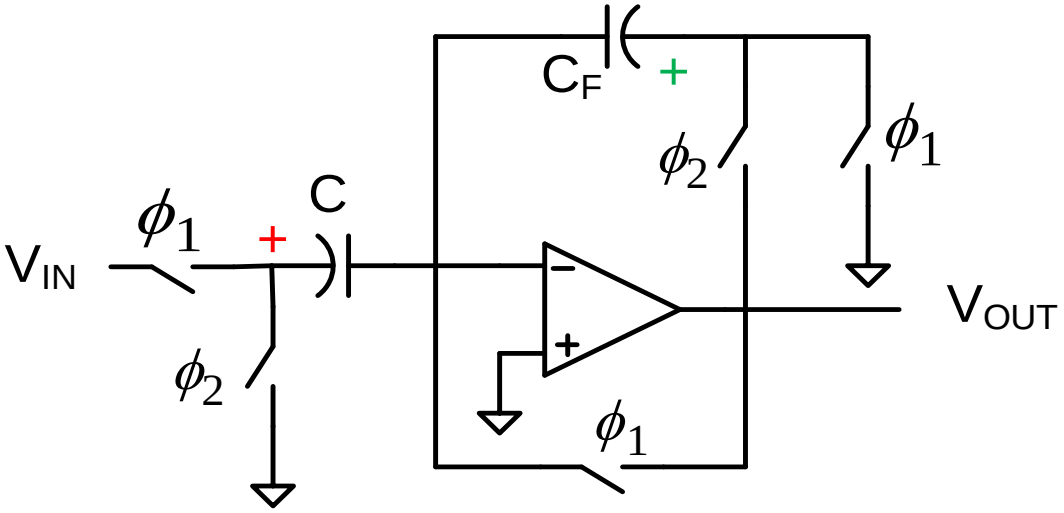
C_X does some good things
(mitigates V_{OS}, 1/f noise and finite gain errors)

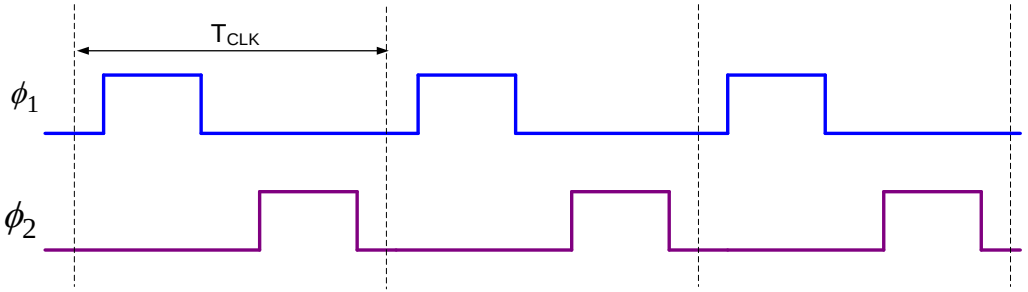
Consider basic charge redistribution circuit



Clocks are complimentary non-overlapping

Basic charge redistribution circuit





During phase φ_1

$$Q_{\phi 1} = CV_{IN}$$

$$Q_{CF} = 0$$

During phase φ_2

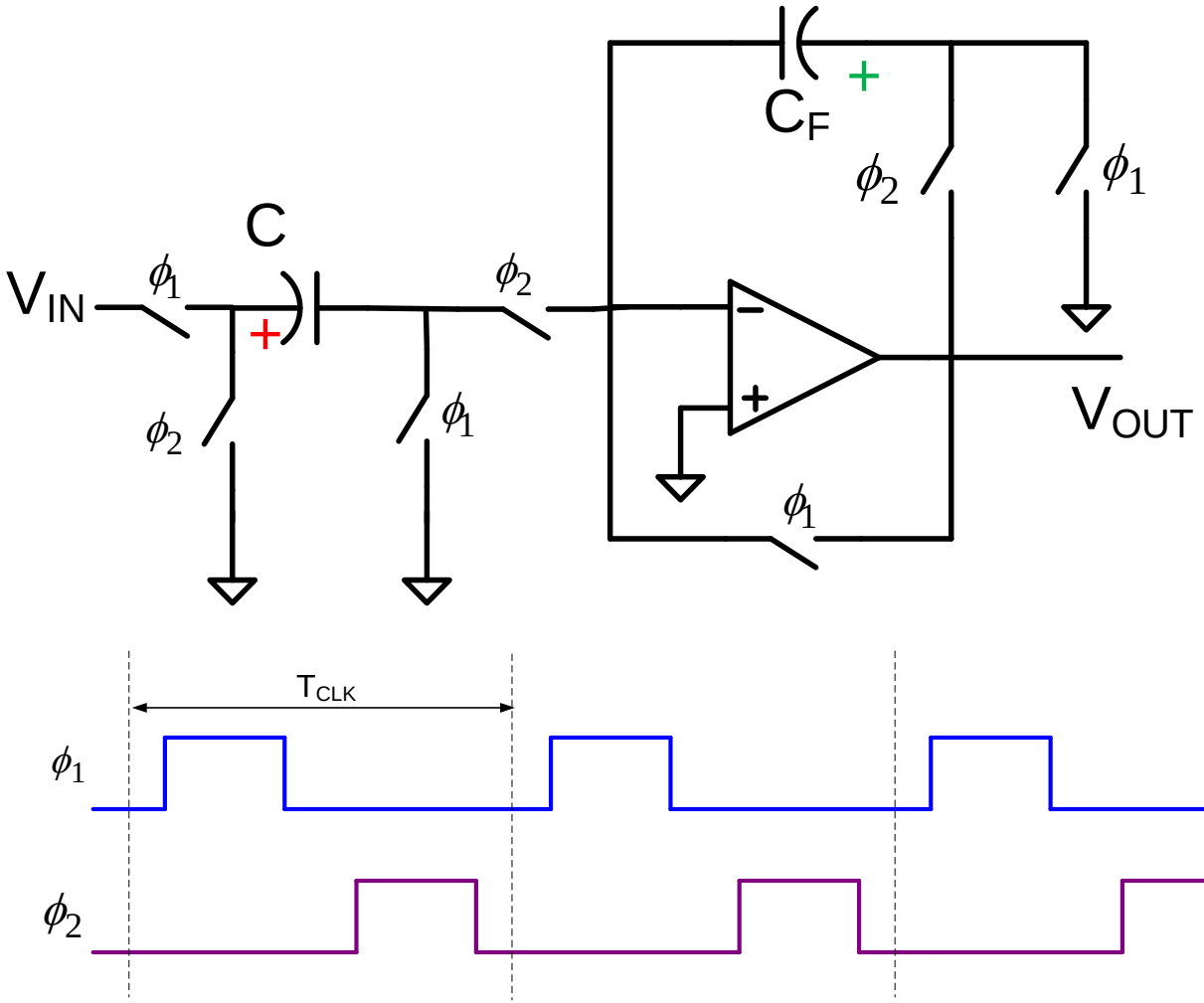
$$\frac{Q_{\phi 1}}{C_F} = V_{OUT}$$

$$\frac{CV_{IN}}{C_F} = V_{OUT}$$

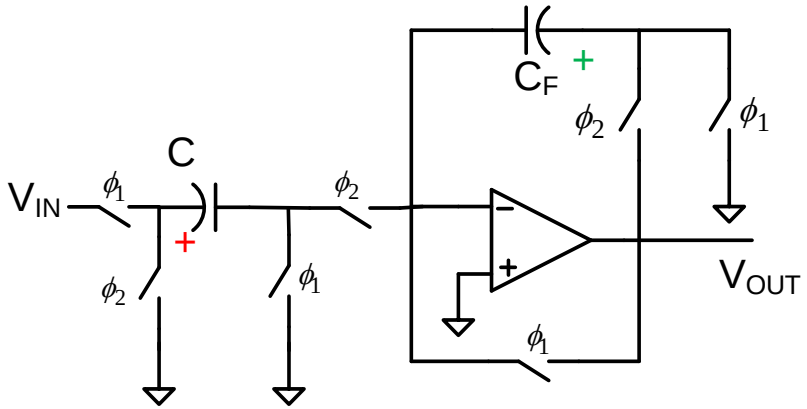
$$\frac{V_{OUT}}{V_{IN}} = \frac{C}{C_F}$$

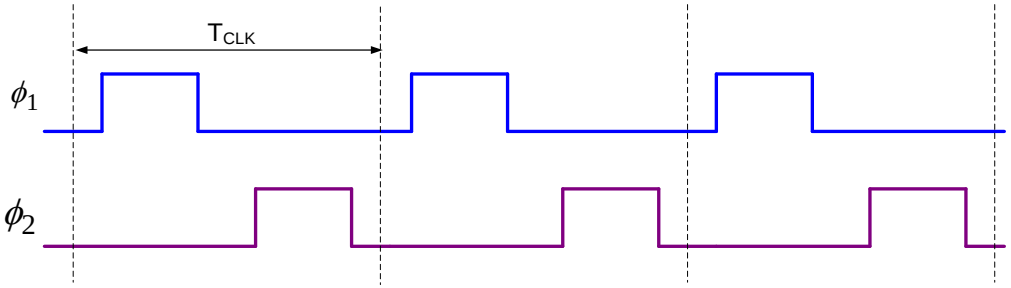
Serves as a noninverting amplifier
Gain can be very accurate
Output valid only during Φ_2

Another charge redistribution circuit



Another charge redistribution circuit





During phase φ_1

$$Q_{\phi 1} = CV_{IN}$$

$$Q_{CF} = 0$$

During phase φ_2

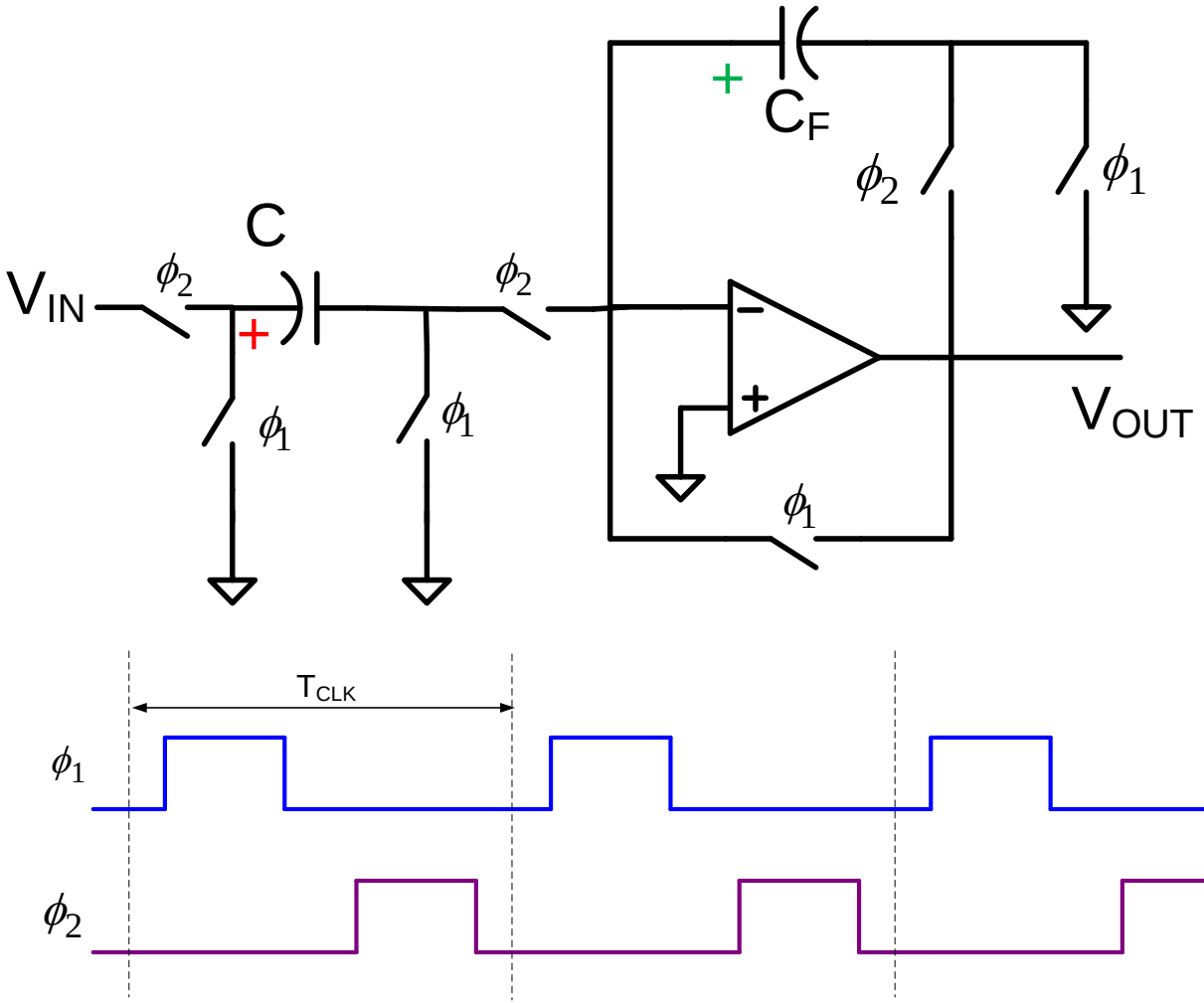
$$\frac{-Q_{\phi 1}}{C_F} = V_{OUT}$$

$$\frac{-CV_{IN}}{C_F} = V_{OUT}$$

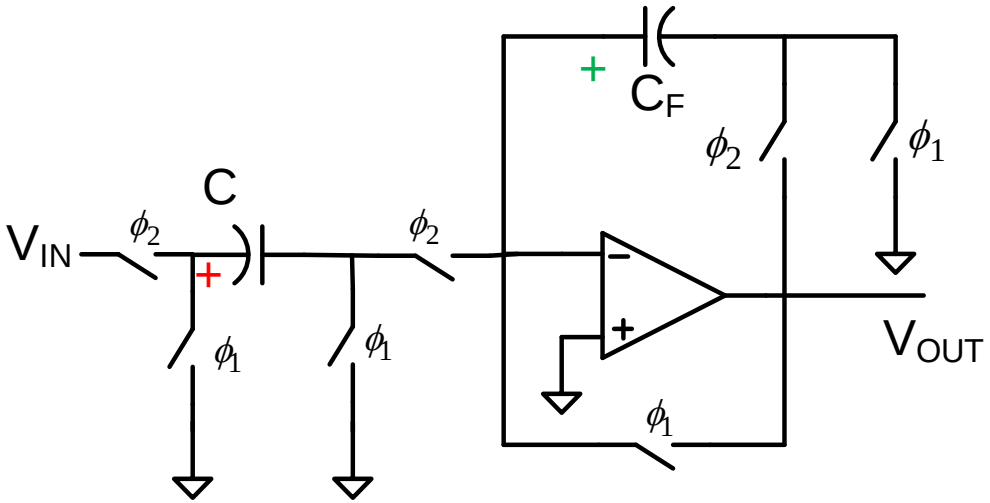
$$\frac{V_{OUT}}{V_{IN}} = -\frac{C}{C_F}$$

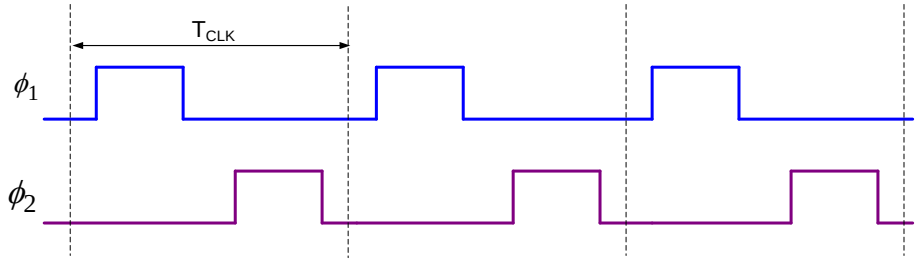
Serves as a noninverting amplifier
Gain can be very accurate
Output valid only during Φ_2

Another charge redistribution circuit



Another charge redistribution circuit





During phase φ_1

$$Q_{\phi 1} = 0$$

$$Q_{CF} = 0$$

During phase φ_2

$$Q_{\phi 2} = CV_{IN}$$

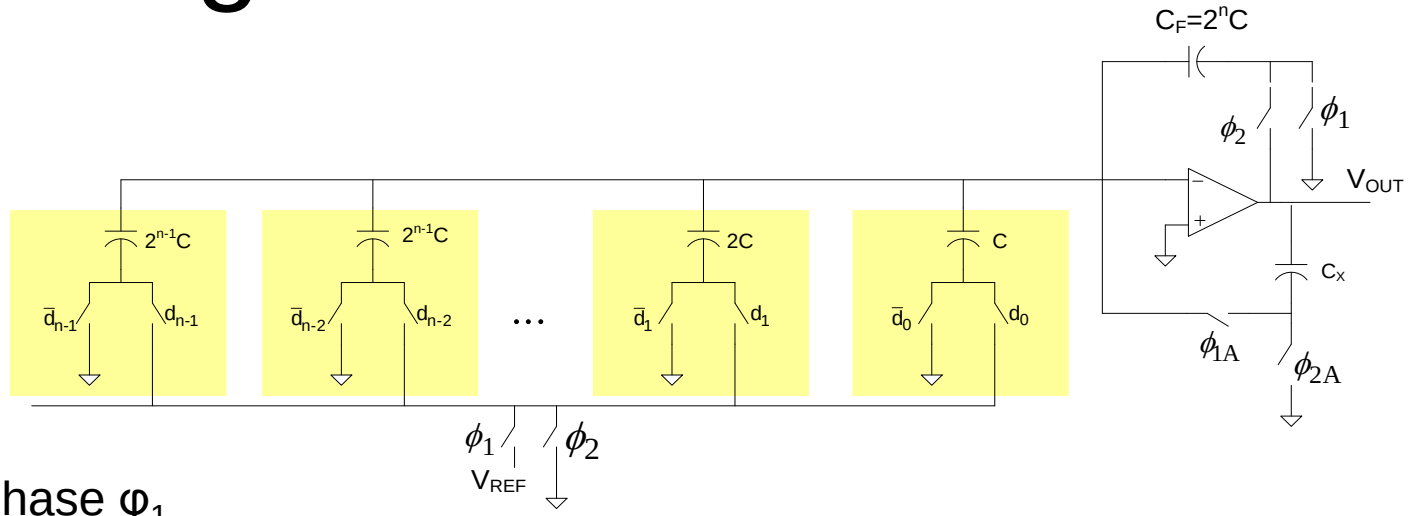
$$Q_{CF} = C_F V_{OUT}$$

$$Q_{CF} = -Q_{\phi 2}$$

$$\frac{V_{OUT}}{V_{IN}} = -\frac{C}{C_F}$$

Serves as a inverting amplifier
Gain can be very accurate
Output valid only during Φ_2

Charge Redistribution DAC



During phase φ_1

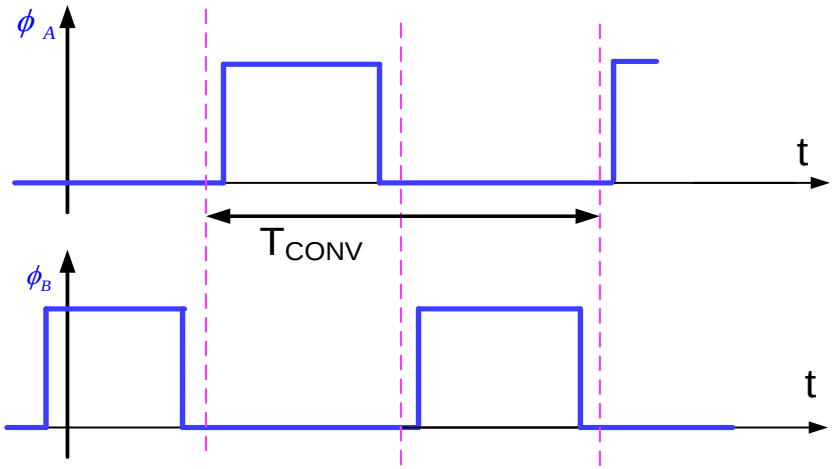
$$Q_{SET} = V_{REF} \sum_{i=0}^{n-1} d_i 2^i C$$

During phase φ_2

Charge Q_{SET} is all transferred to C_F

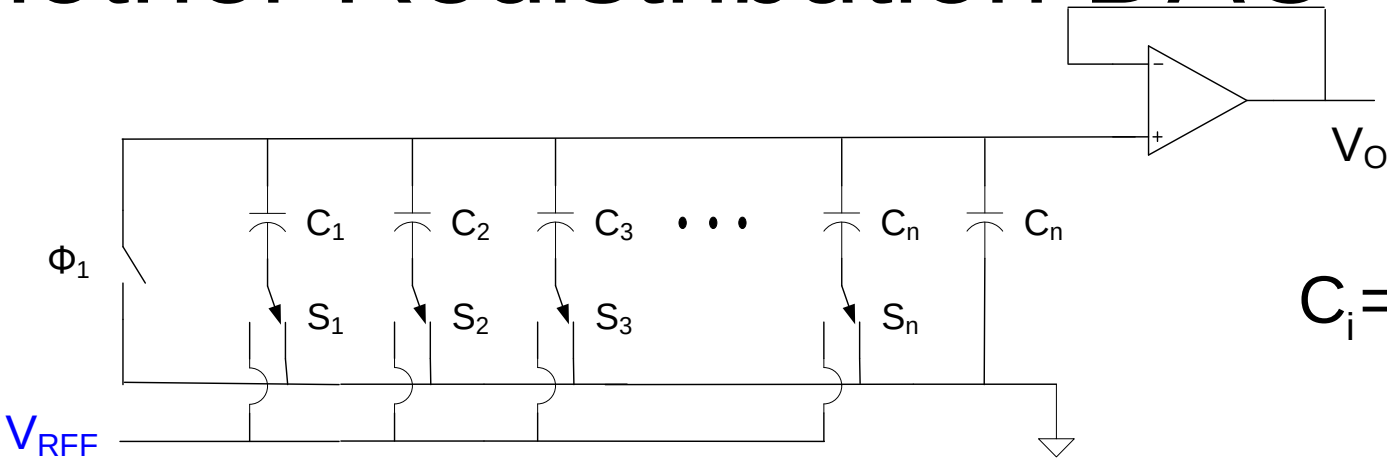
$$Q_{CF} = V_{OUT} 2^n C$$

but $Q_{SET} = Q_{CF}$



$$V_{REF} \sum_{i=0}^{n-1} d_i 2^i C = V_{OUT} 2^n C \Rightarrow V_{OUT} = V_{REF} \sum_{i=0}^{n-1} \frac{d_i}{2^{n-i}}$$

Another Redistribution DAC



$$C_i = \frac{C}{2^i}$$

During phase φ_1 selected switches set to V_{REF}

$$Q_{SET} = V_{REF}\sum_{i=0}^{n} d_i C_i = V_{REF}\sum_{i=0}^{n} d_i \frac{C}{2^{n-i}}$$

During phase φ_2 all switches connected to GND

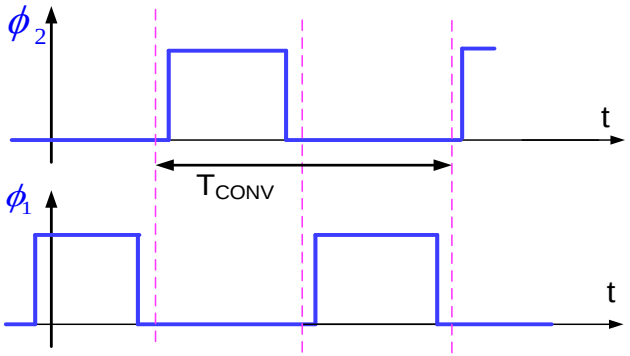
Charge Q_{SET} is all redistributed among the capacitors

$$Q_{SET} = V_{OUT}\left(\sum_{i=1}^{n} C_i + C_n\right)$$

but

$$\sum_{i=1}^{n} C_i + C_n = \left(\sum_{i=1}^{n} \frac{C}{2^i} + C_n\right) = C$$

$$Q_{SET} = V_{OUT} C$$



$$V_{REF}\sum_{i=0}^{n-1} d_i \frac{C}{2^{n-i}} = V_{OUT} C \quad \Rightarrow \quad V_{OUT} = V_{REF}\sum_{i=0}^{n-1} \frac{d_i}{2^{n-i}}$$

Stay Safe and Stay Healthy !

End of Lecture 17